

Compal Confidential

BIZ00 M/B Schematic Document

Intel Skylake Y Processor

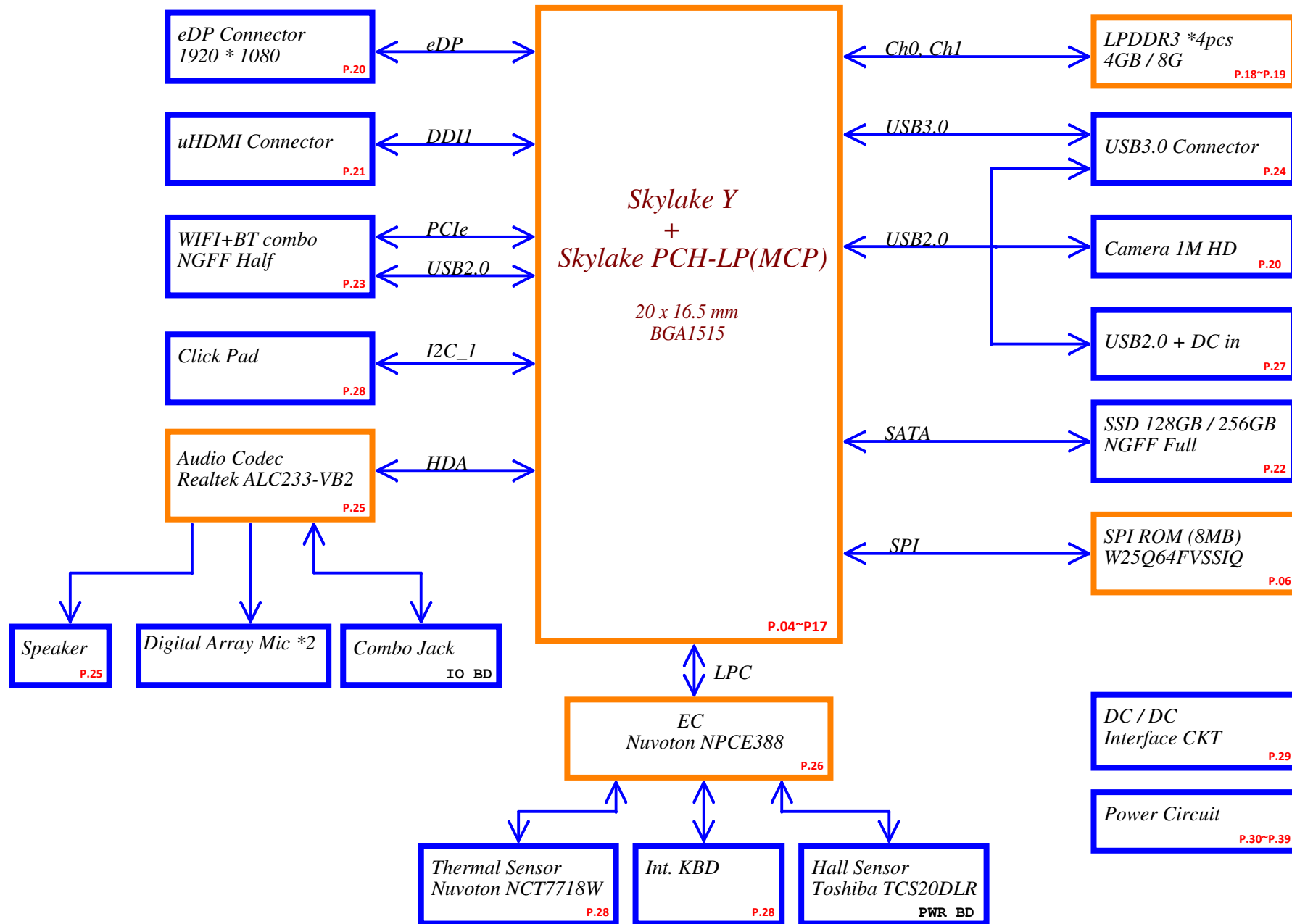
LA-D341P

2015-09-01

REV: 0.3

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Intel Skylake Y Block Diagram



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Voltage Rails

power plane	State	B+	+5VALW +3VALW +1.8VALW +1.0VALW	+1.2V_VDDQ +1.8V_MEM +1.0VS_VCCST +1.0VS_VCCIO +VCC_CORE +VCC_GT +VCC_SA +0.6VS_VTT	+5VS +3VS +1.8VS +1.0VS_VCCSTG +1.0VS_VCCIO +VCC_CORE +VCC_GT +VCC_SA +0.6VS_VTT
S0		O	O	O	O
S3		O	O	O	X
S5 S4/AC		O	O	X	X
S5 S4/ Battery only		X	X	X	X
S5 S4/AC & Battery don't exist		X	X	X	X

EC SM Bus1 address

EC SM Bus2 address

Device	Address	Device	Address
Smart Battery		Thermal Sensor NCT7718W	1001100x
Charger		Skylake Y SML1	

CPU SM Bus address

CPU SML0 Bus address

Device	Address	Device	Address
NA		NA	

SMBUS Control Table

	HOST	Changer	BATT	NPCE388	CPU	Thermal sensor NCT7718W
EC_SMB_CK1 EC_SMB_DA1	NPCE388 +3VLP	V +3VLP	V +3VLP	X	X	X
EC_SMB_CK2 EC_SMB_DA2	NPCE388 +3VS	X	X	X	V +3VS	V +3VS
SMBCLK SMBDATA	CPU +3VALW	X	X	X	X	X
SML0CLK SML0DATA	CPU +3VALW	X	X	X	X	X
SML1CLK SML1DATA	CPU +3VS	X	X	V +3VS	X	V +3VS

STATE	SIGNAL	SLP_S0#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB 2.0 Port Table

USB 2.0	Port	3 External USB Port
	1	USB 3.0/2.0 Port (MB)
	2	
	3	Camera
	5	BT
	7	
	9	DCIN-USB

USB 3.0 Port Table

Port	
1	USB 3.0 Port (MB)
2	
3	
4	

SATA Port Table

Port	
0	
1	NGFF SSD(SATA)
2	
3	

PCIE Port Table

Port	Lane	
1		
2		
3		
4		
5	0	
	1	
	2	
	3	
6		NGFF WLAN

BOM Structure Table

BTO Item	BOM Structure
Connector	ME@
76 LEVEL	X76@
UNPOP	@
CPU OPTION	
DRAM Option	S4G@ H4G@ M4G@ S8G@ H8G@ M8G@
EMI POP	EMI@
ESD POP	ESD@
RF POP	RF@
EMI UNPOP	@EMI@
ESD UNPOP	@ESD@
45 LEVEL	45@

HDMI Logo



HDMI Logo
R00000003HM

DRAM



MICRON
X7665538L01

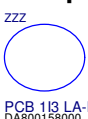
EDF8132A3MA-JD-F-R
SA00008PF00



SAMSUNG
X7665538L02

K4E8E304EE-EGCFT00
SA00008PF00

PCB part



PCB 113 LA-D341P REV0 M/B
DA600158000



MICRON
X7665538L03

EDFA232A2MA-JD-F-R
SA00008Q100



SAMSUNG
X7665538L04

K4E6E304EE-EGCFT00
SA00008Q100

CPU part



SR2EN D1 0.9G
SA000092Y40



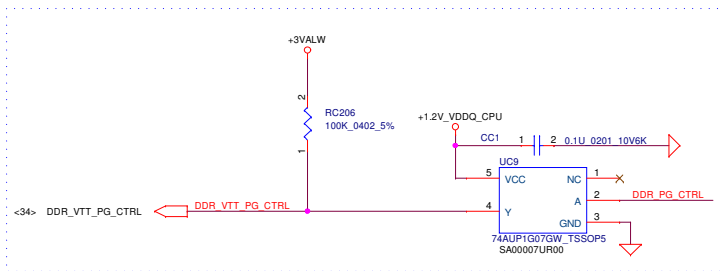
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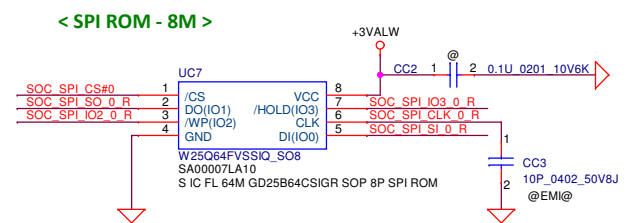
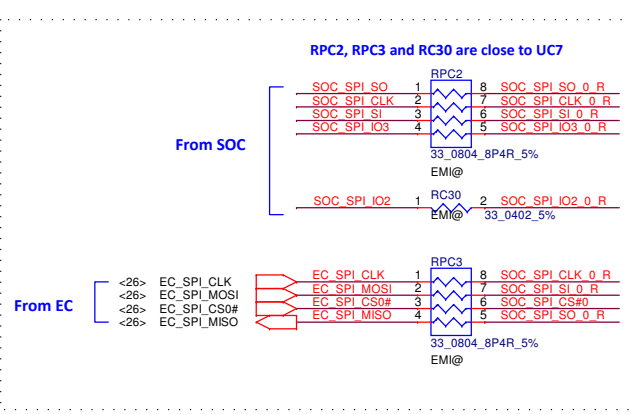
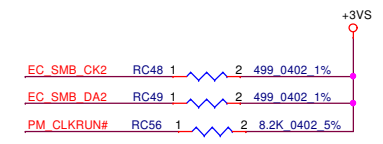
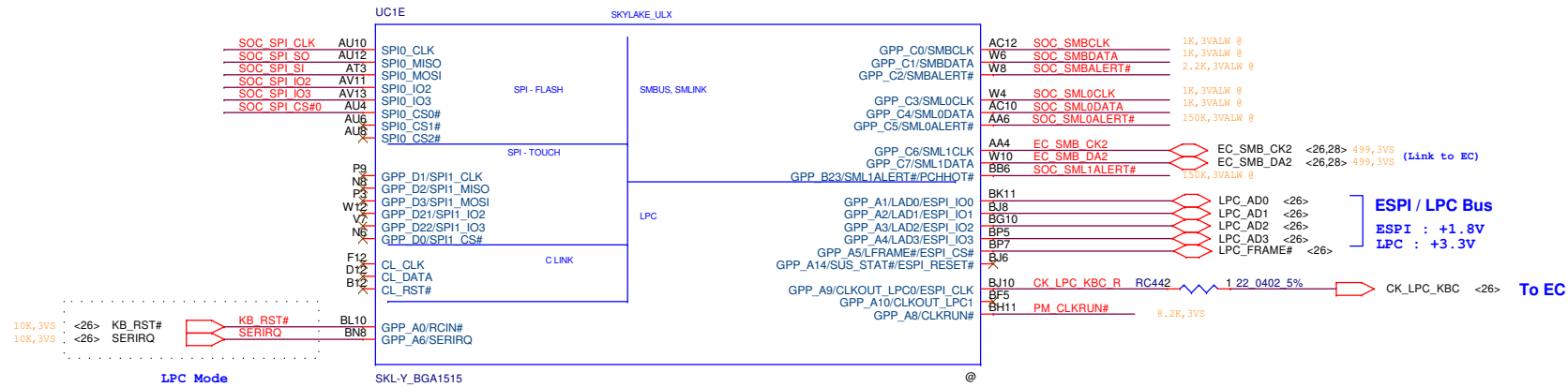


SR2EH D1 1.2G
SA000092V40

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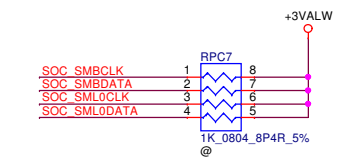
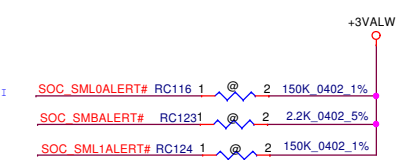
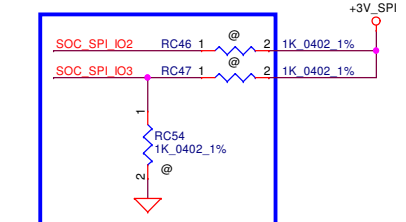
Vinafix.com



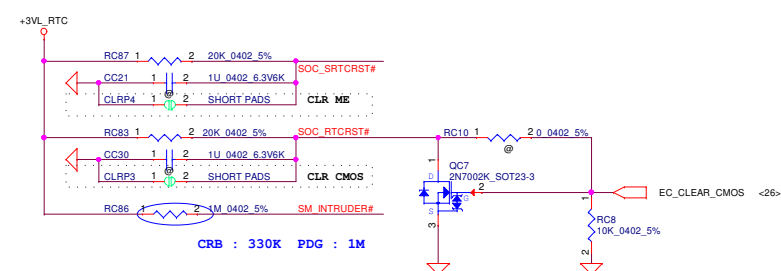
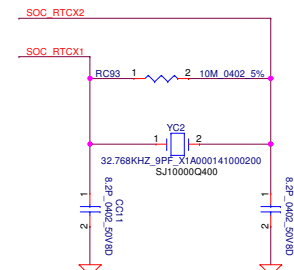
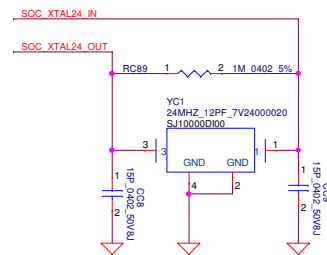
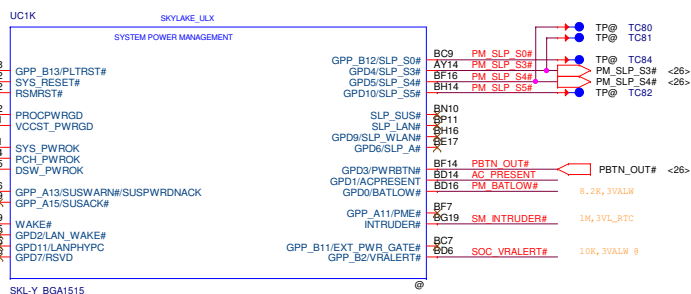
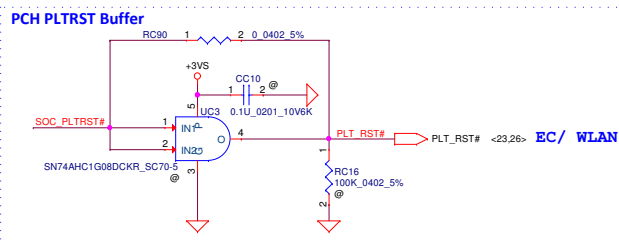
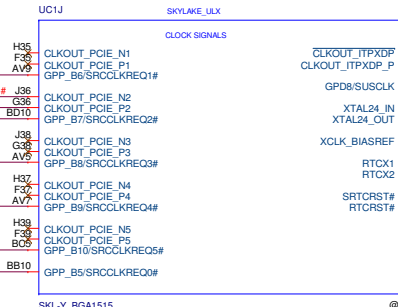
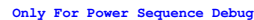


follow MOW 6 & 9 rev 1.0
omit any PU/PD

default internal PD for LPC, PU for eSPI



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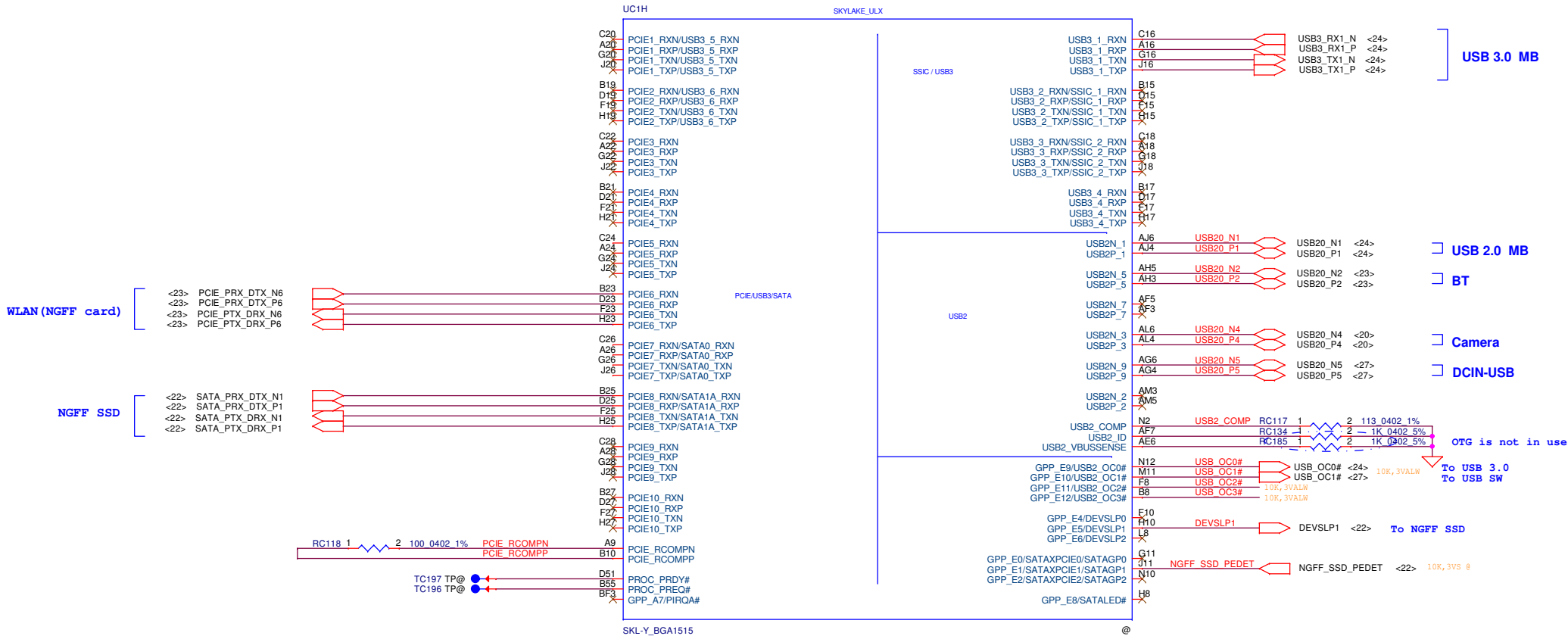
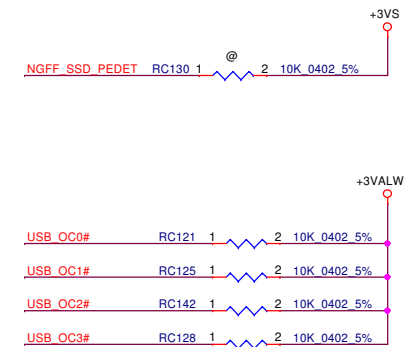
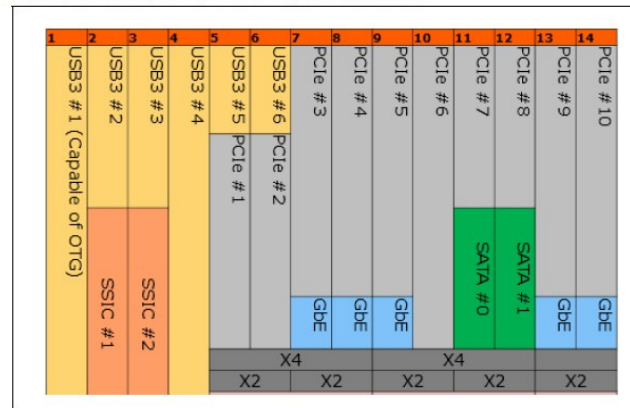
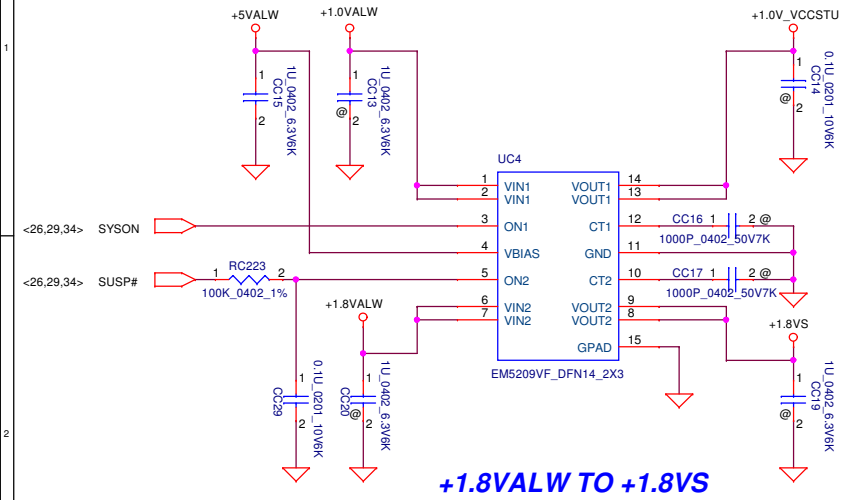


Figure 11-2. High Speed I/O (HSIO) Lane Multiplexing in SKL Y

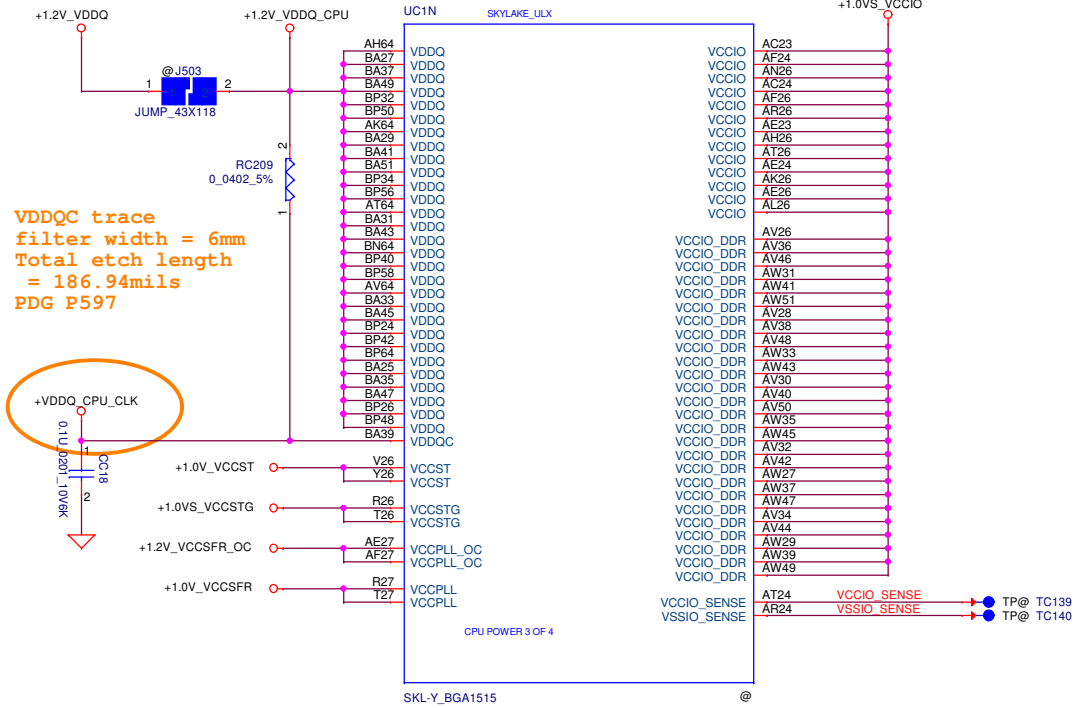


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+1.0VALW TO +1.0V_VCCSTU

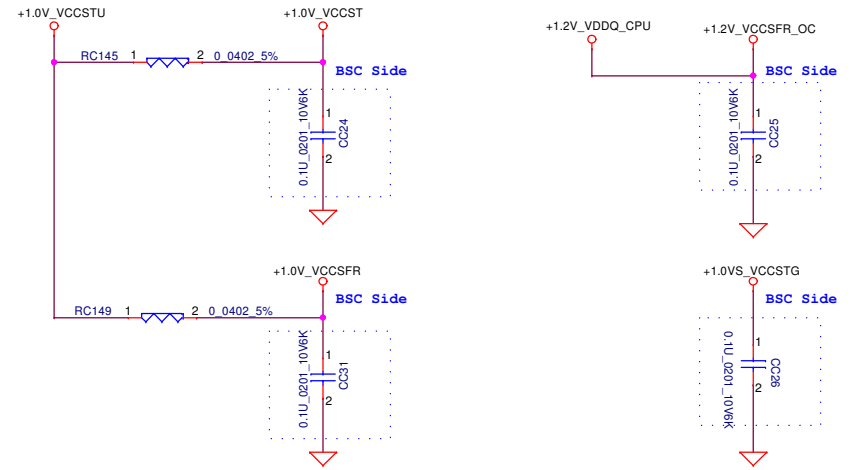
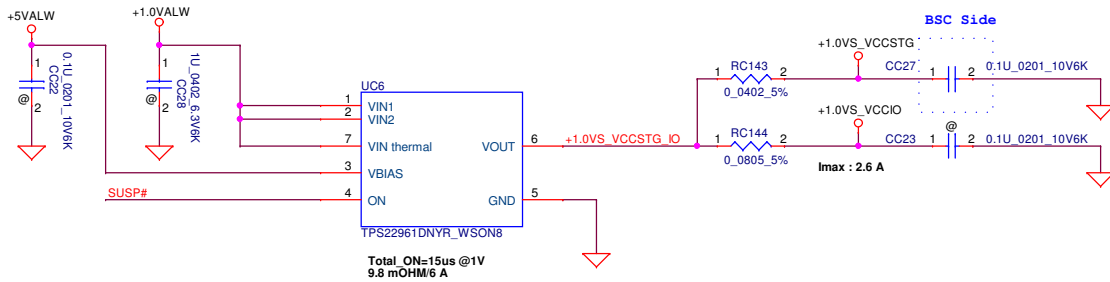


+1.8VALW TO +1.8VS

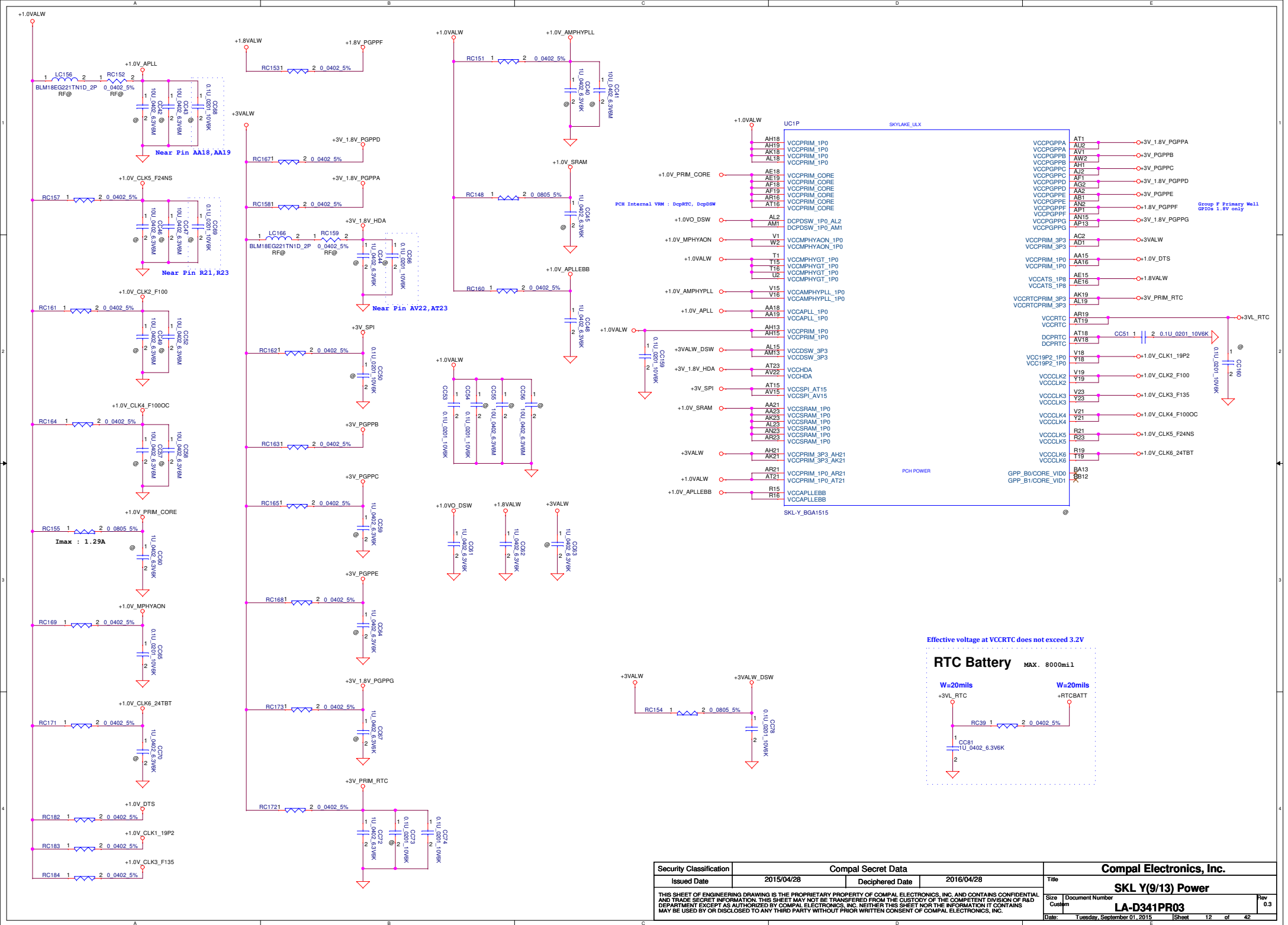


VDDQC trace
filter width = 6mm
Total etch length
= 186.94mils
PDG P597

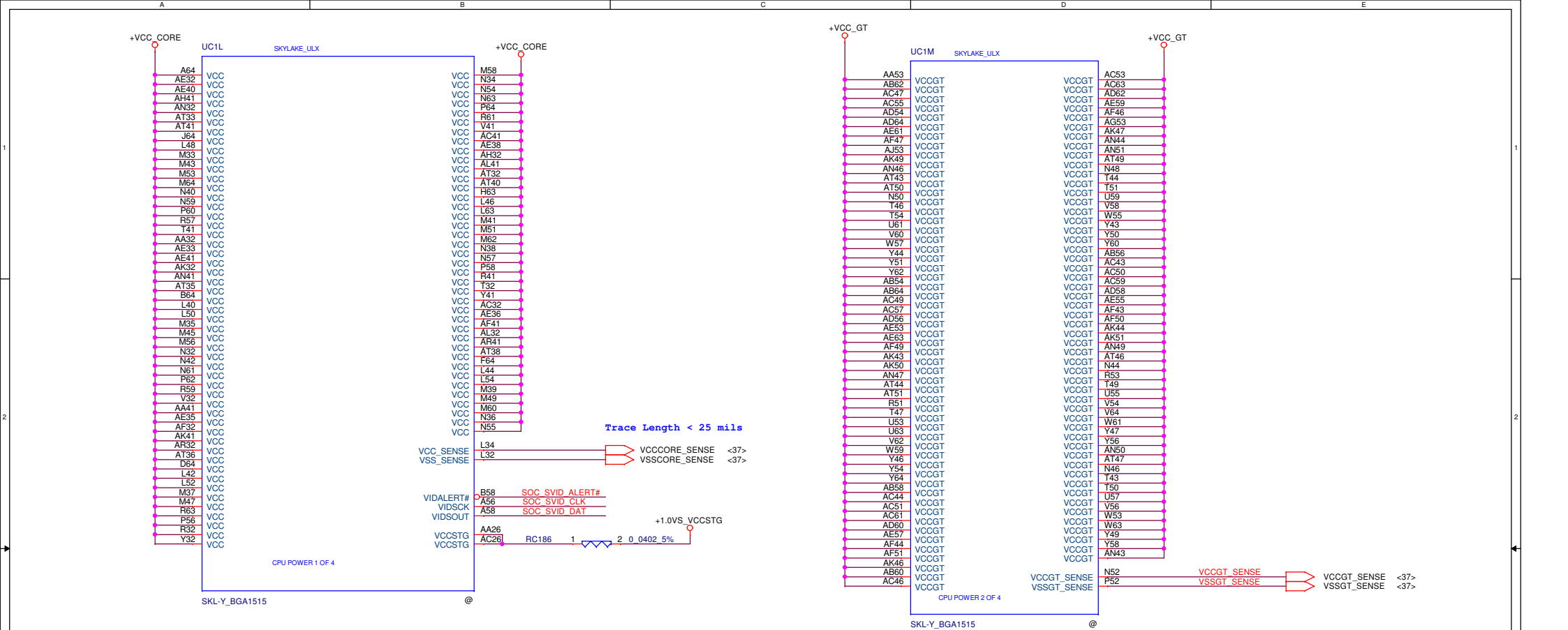
+1.0VALW TO +1.0VS_VCCSTG / +1.0VS_VCCIO



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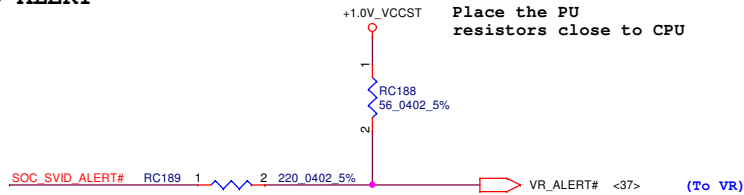


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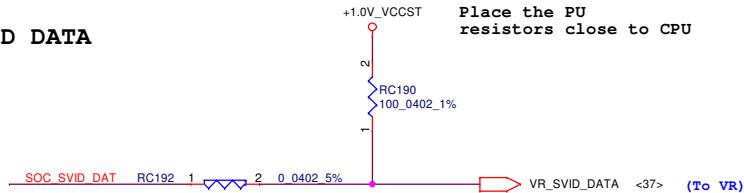
SVID ALERT

Place the PU resistors close to CPU



SVID DATA

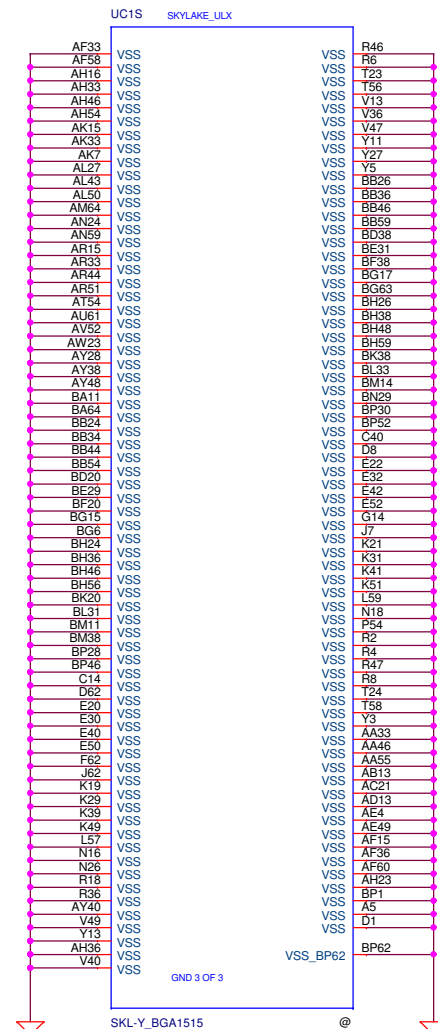
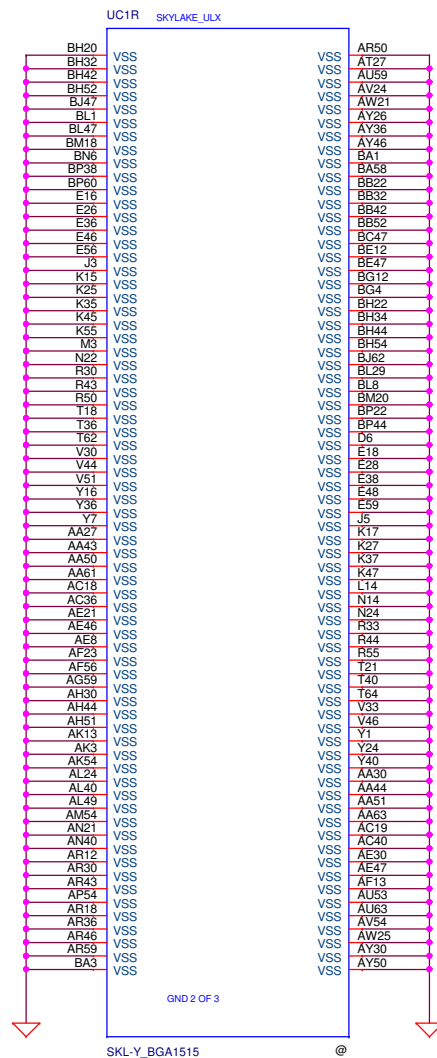
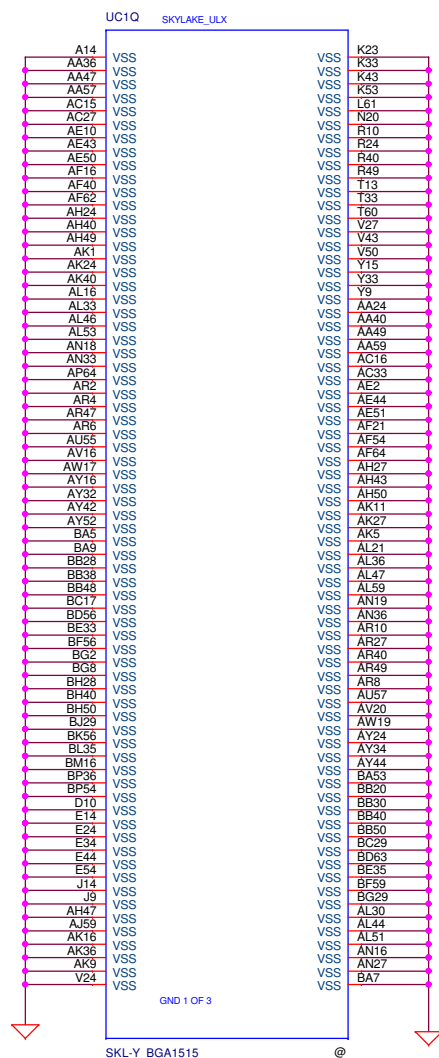
Place the PU resistors close to CPU



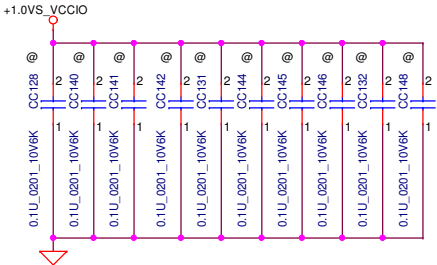
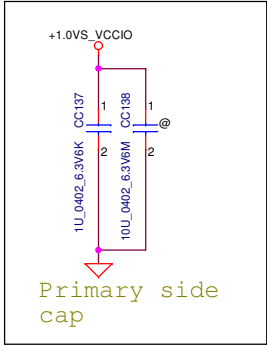
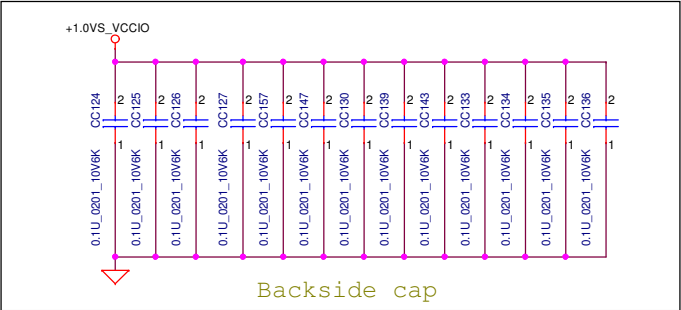
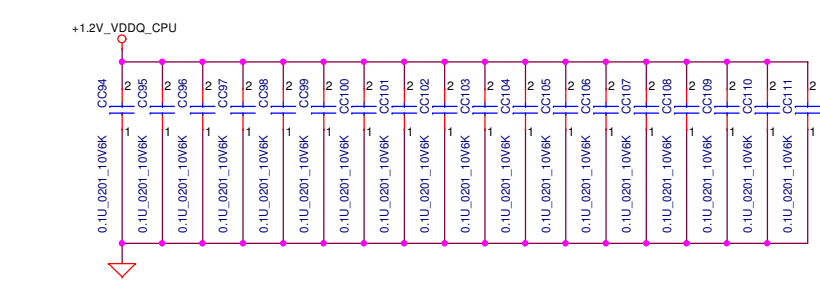
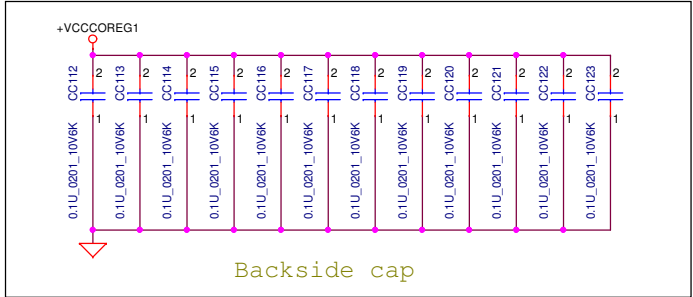
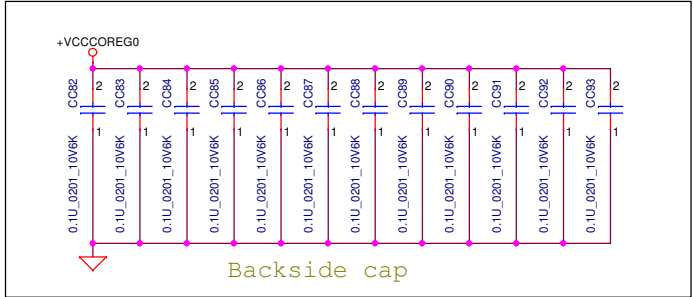
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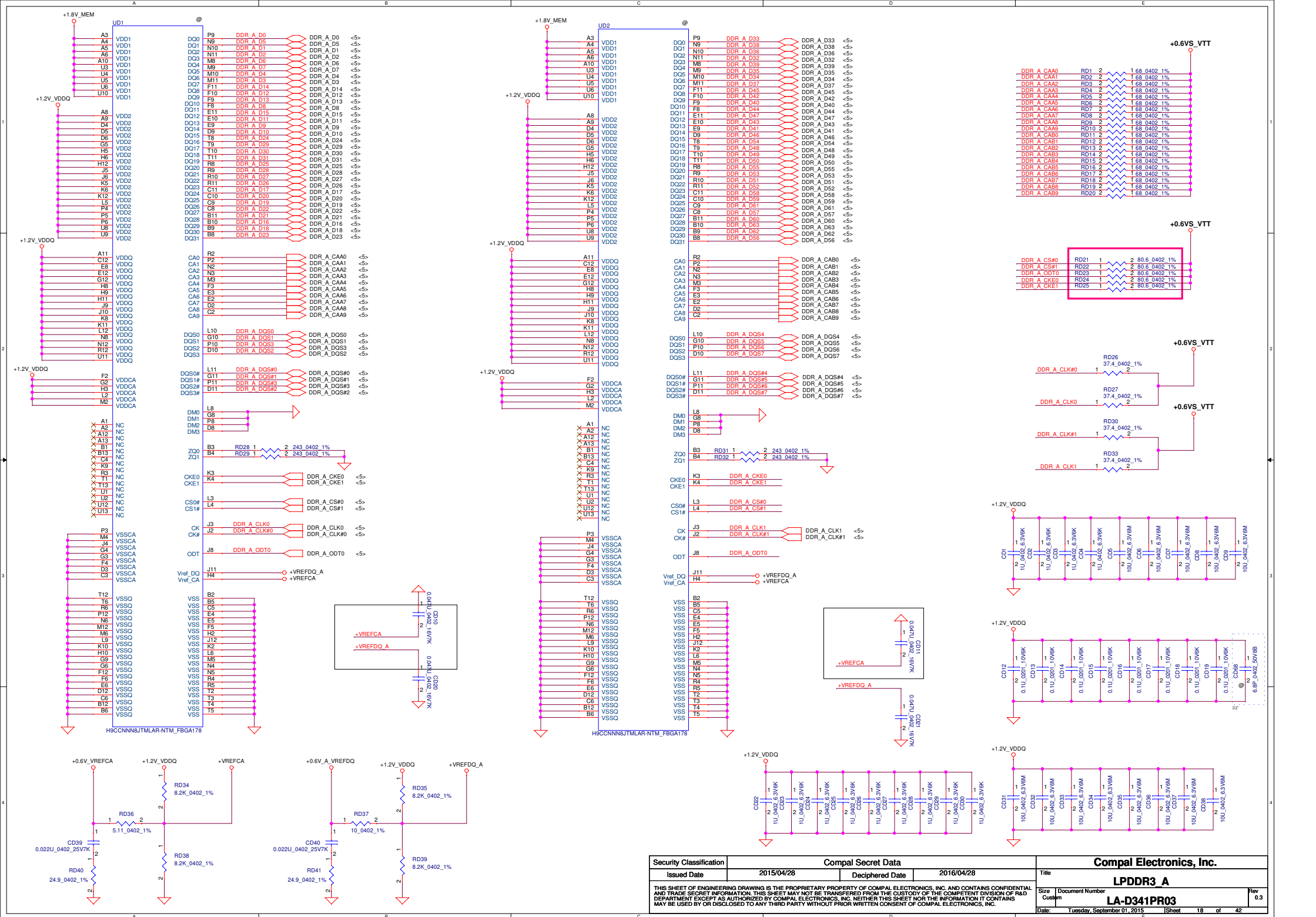
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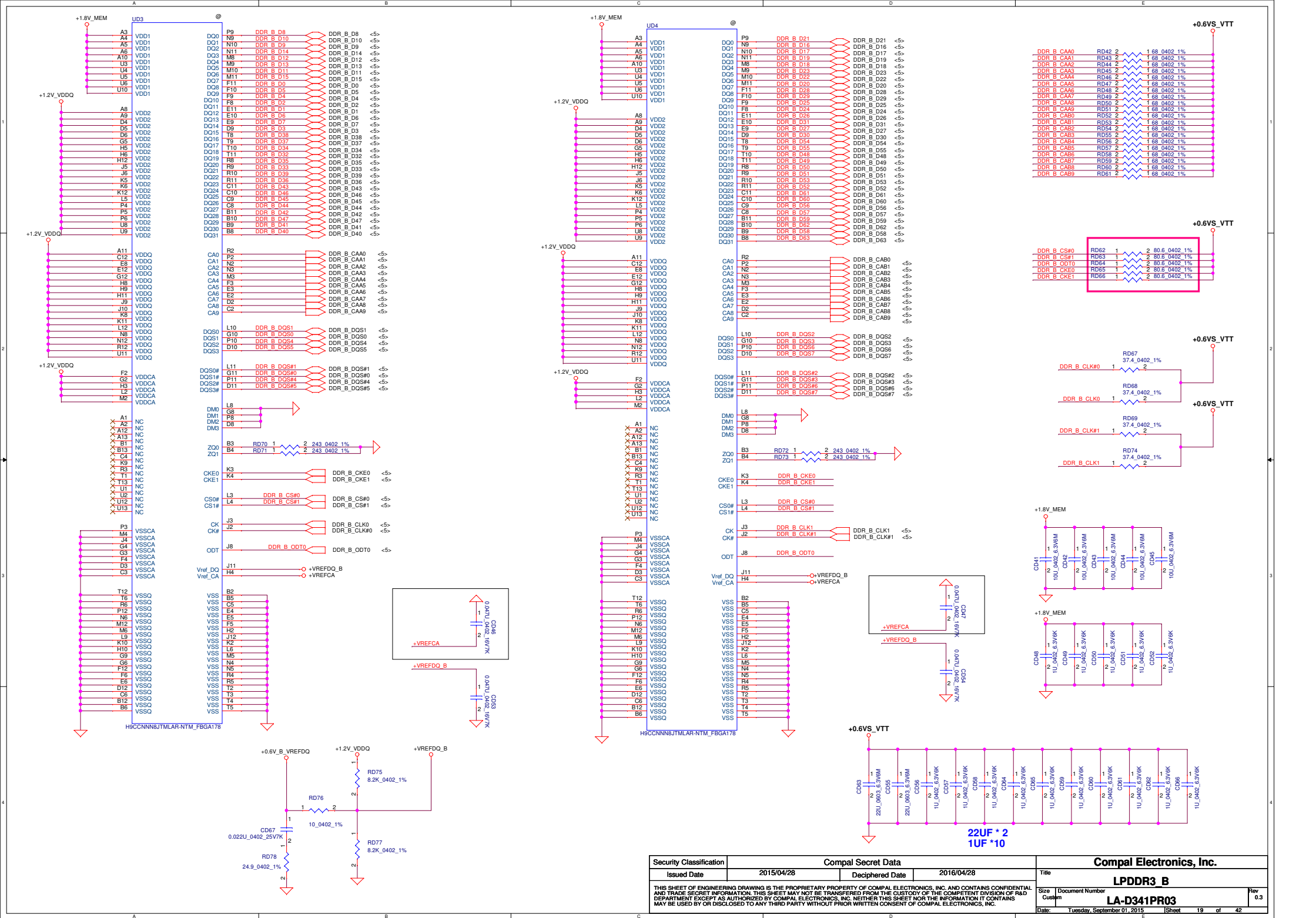


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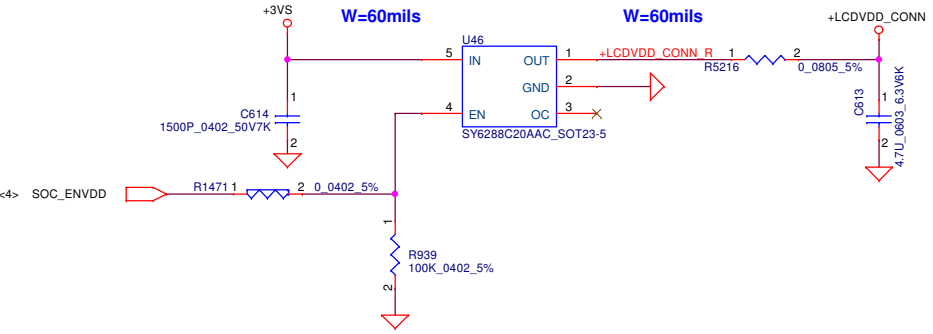


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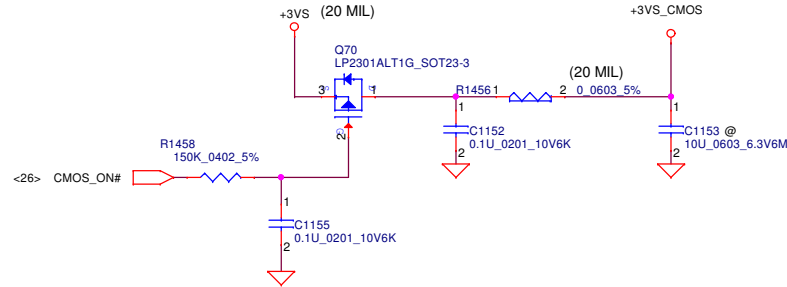




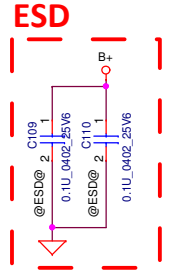
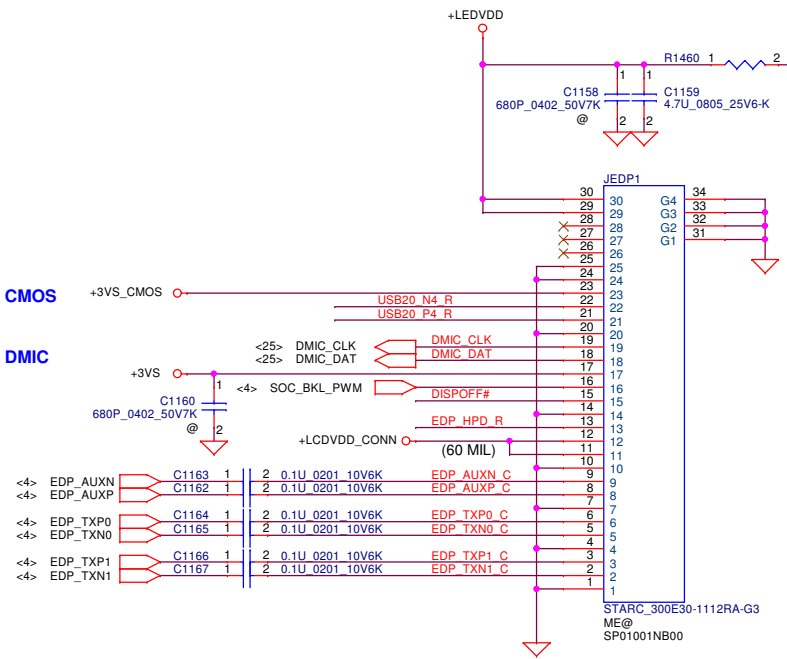
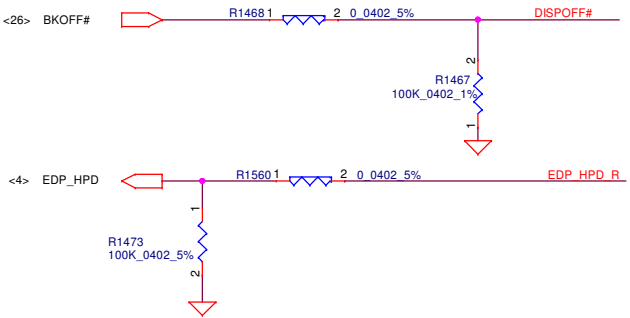
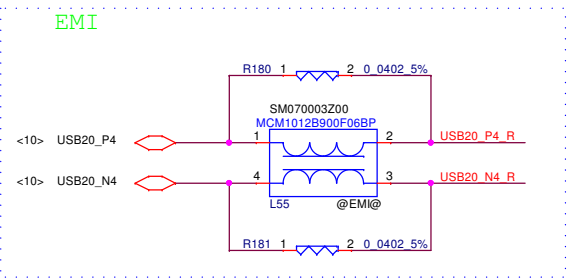
LCD POWER CIRCUIT



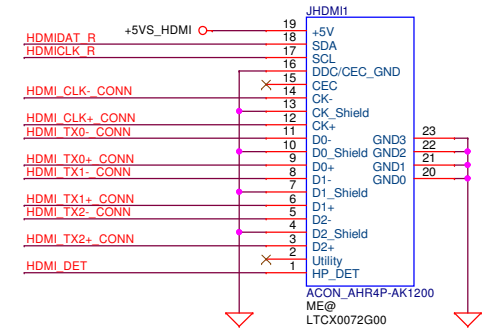
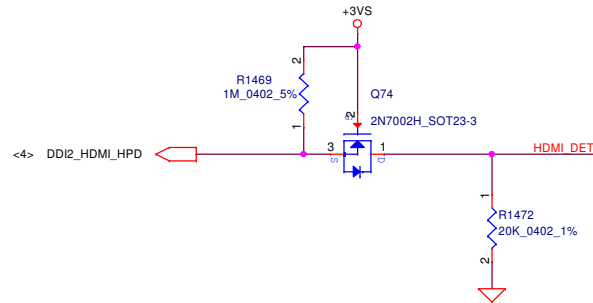
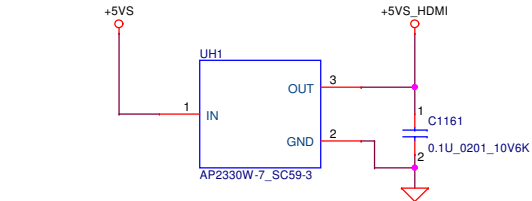
CMOS Camera



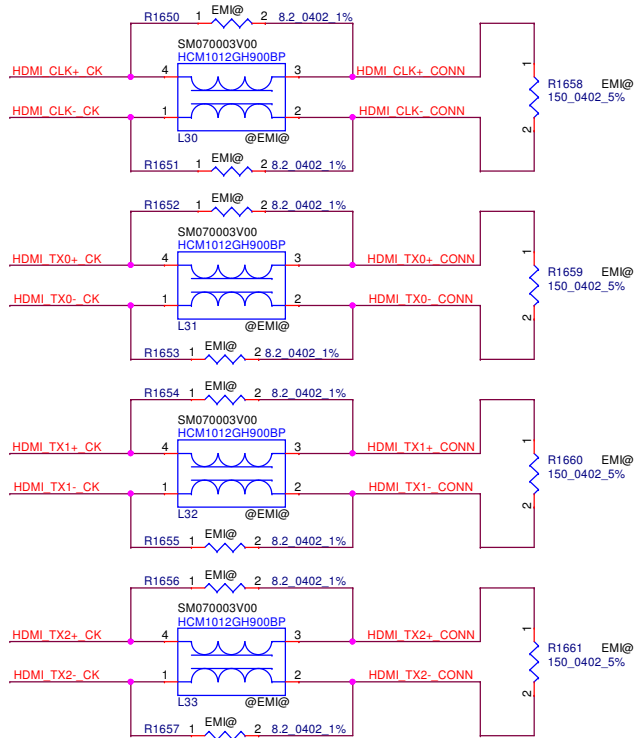
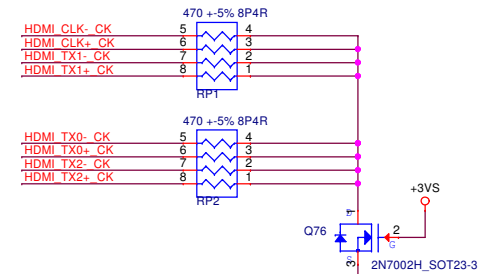
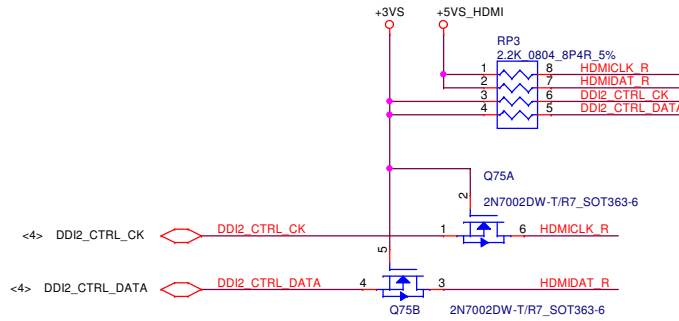
eDP PANEL/DMIC/COMS Conn.



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Size	Custom	Document Number	LA-D341PR03	Rev	0.3
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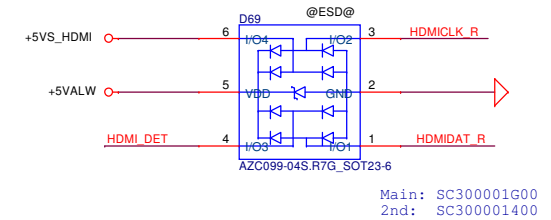
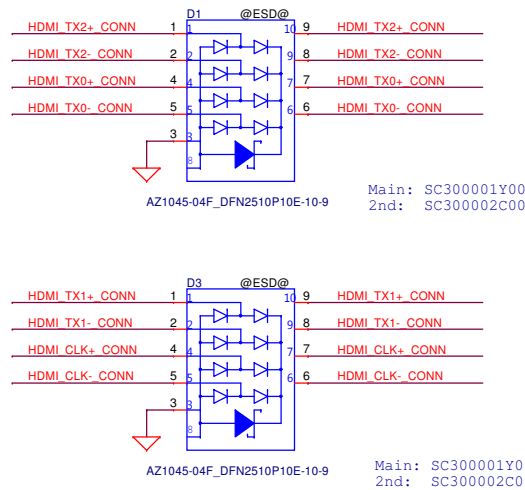


<4>	CPU_DP2_N0	CPU_DP2_N0	0.1U_0201_10V6K	2	1	C46	HDMI_TX2_-CK
<4>	CPU_DP2_P0	CPU_DP2_P0	0.1U_0201_10V6K	2	1	C47	HDMI_TX2+_CK
<4>	CPU_DP2_N1	CPU_DP2_N1	0.1U_0201_10V6K	2	1	C48	HDMI_TX1_-CK
<4>	CPU_DP2_P1	CPU_DP2_P1	0.1U_0201_10V6K	2	1	C55	HDMI_TX1+_CK
<4>	CPU_DP2_N2	CPU_DP2_N2	0.1U_0201_10V6K	2	1	C56	HDMI_TX0_-CK
<4>	CPU_DP2_P2	CPU_DP2_P2	0.1U_0201_10V6K	2	1	C58	HDMI_TX0+_CK
<4>	CPU_DP2_N3	CPU_DP2_N3	0.1U_0201_10V6K	2	1	C72	HDMI_CLK-_CK
<4>	CPU_DP2_P3	CPU_DP2_P3	0.1U_0201_10V6K	2	1	C74	HDMI_CLK+_CK



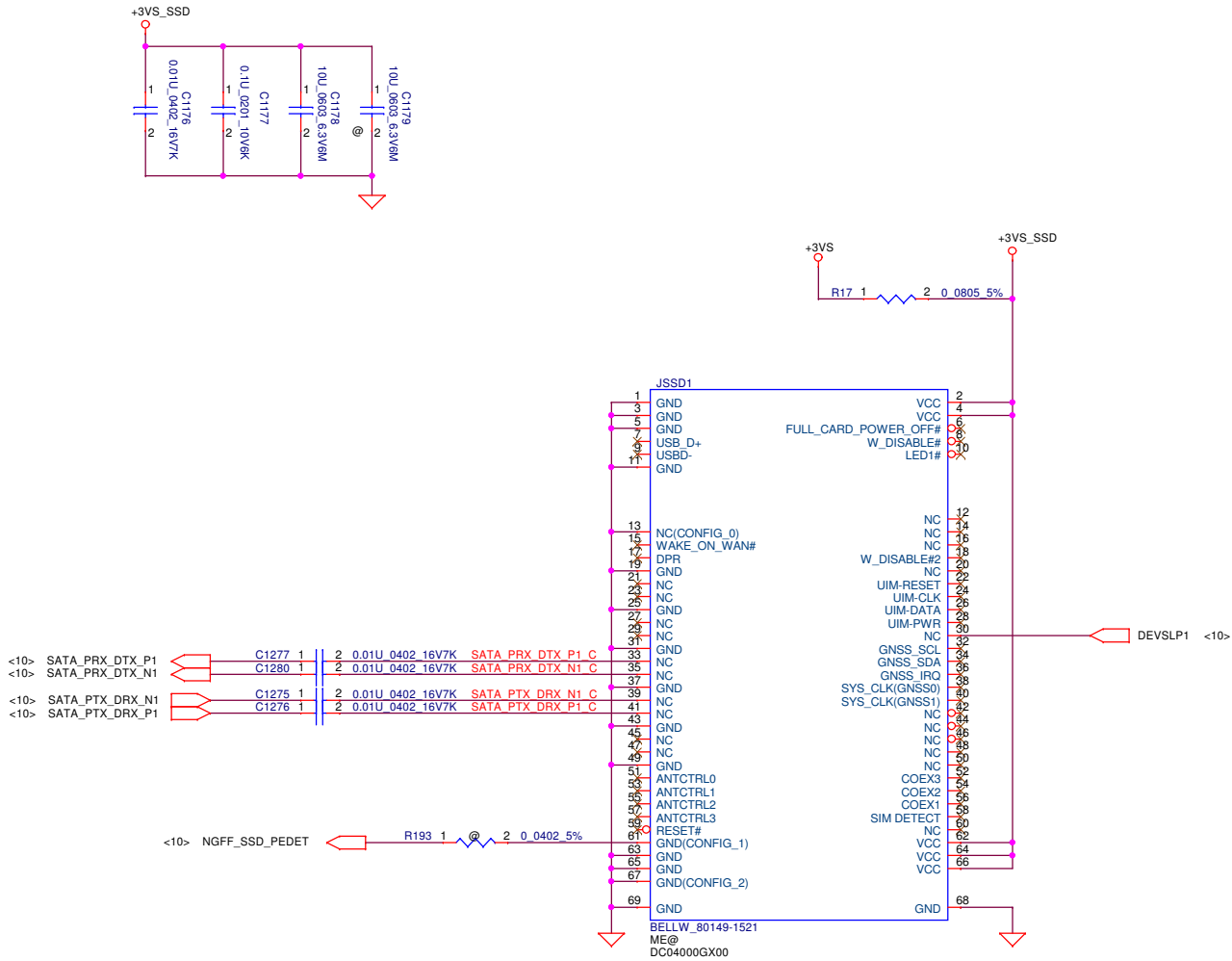
ESD

Close to HDMI connector



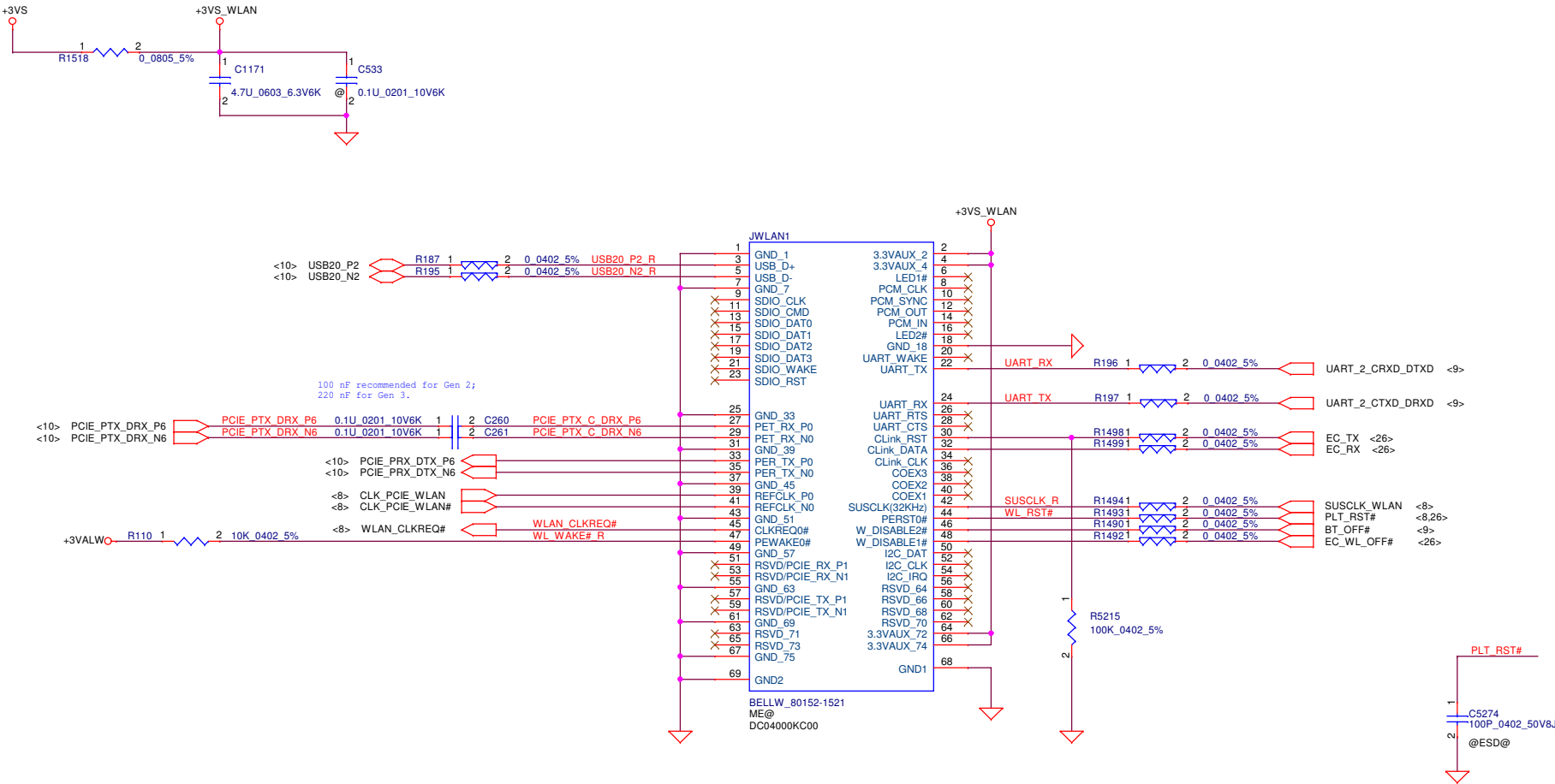
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Issued Date				2015/04/28				Deciphered Date			
2015/04/28				2016/04/28				Title			
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Size				Document Number				Rev			
Custom				LA-D341PR03				0.3			
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NGFF for SSD(Key B)



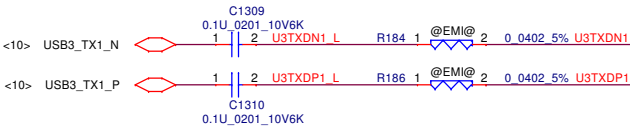
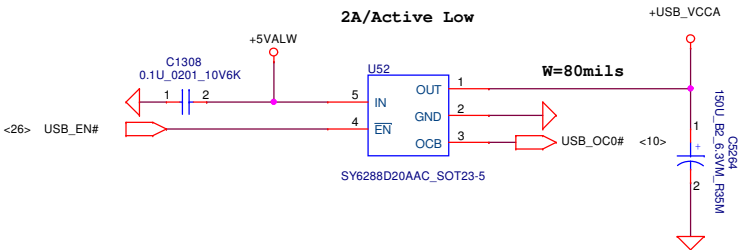
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Size	Custom	Document Number	LA-D341PR03	Rev	0.3
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NGFF for WLAN(Key E)

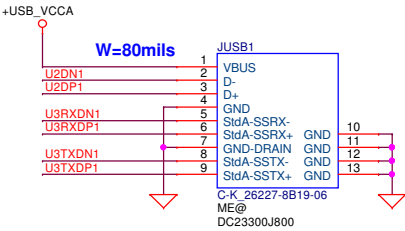
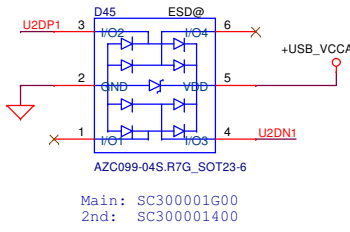
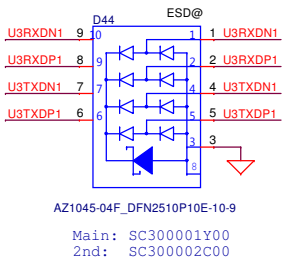


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Size	Custom	Document Number	LA-D341PR03	Rev	0.3
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USB 3.0 Conn.

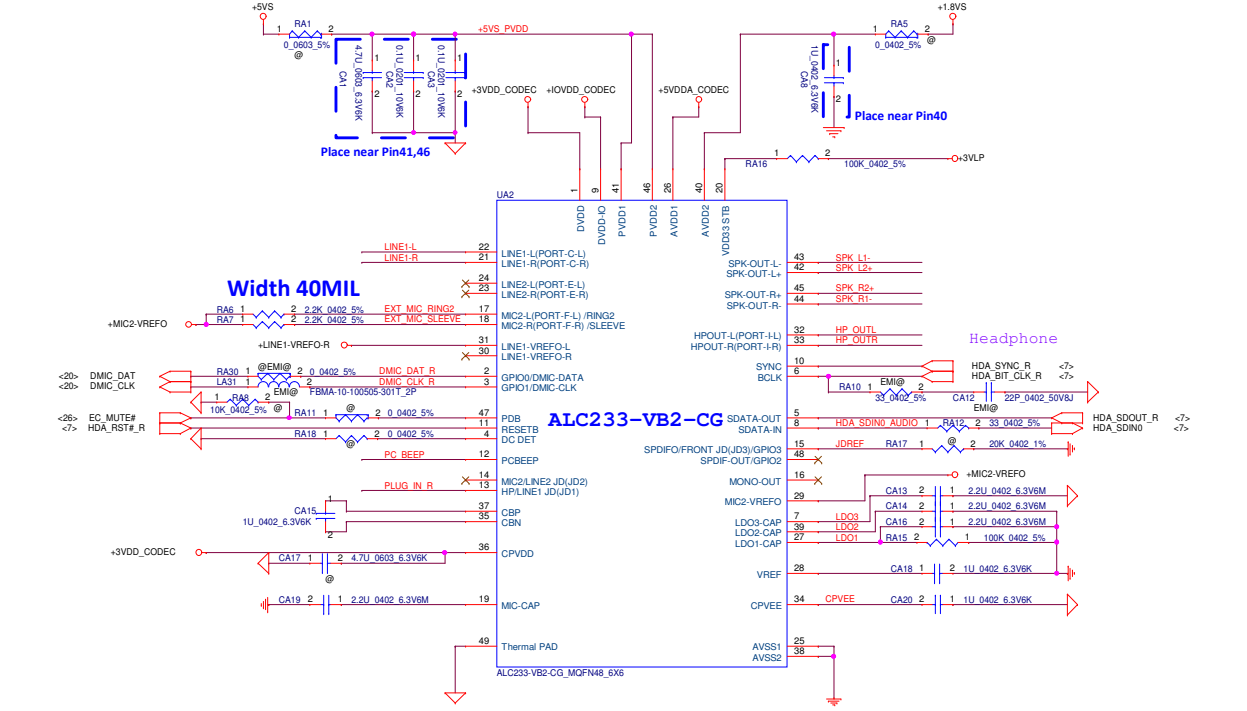


Place TX AC coupling Cap (C843~C850). Close to connector

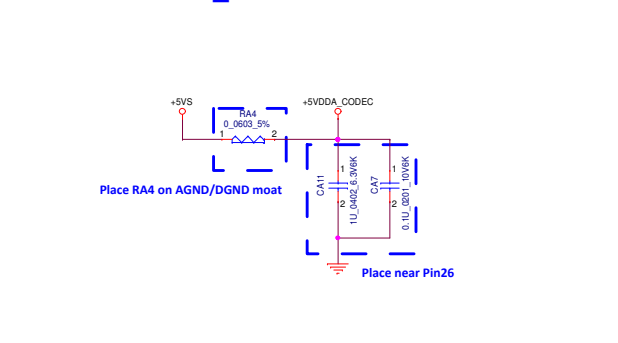


Security Classification				Compal Secret Data				Compal Electronics, Inc.			
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										USB 3.0	
										LA-D341PR03	
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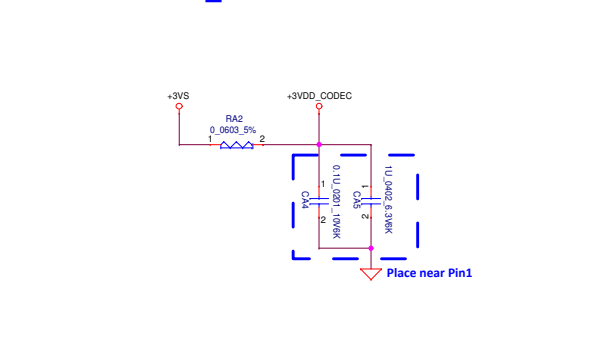
ALC233-VB2



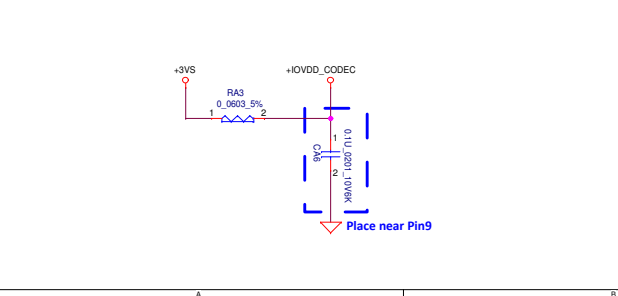
+5VS → +5VDDA_CODEC



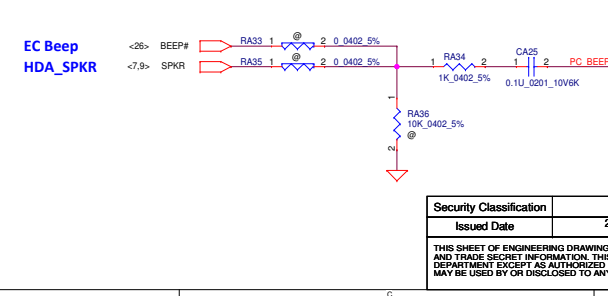
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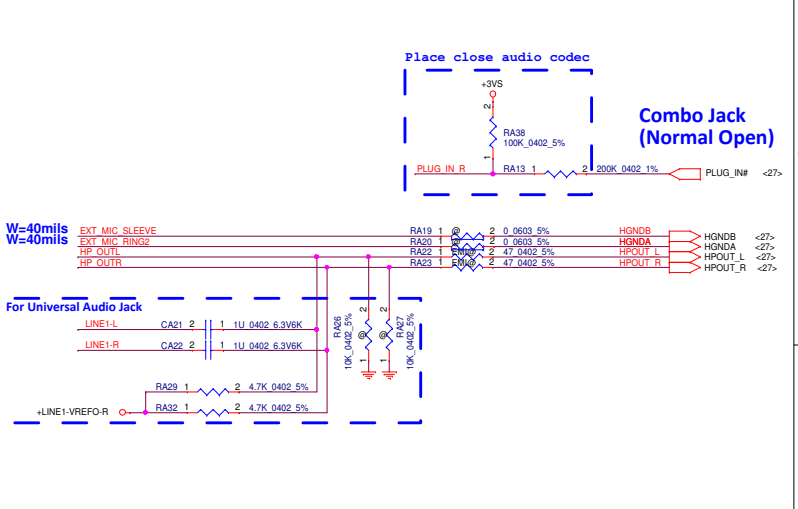
+3VS → +IOVDD_CODEC



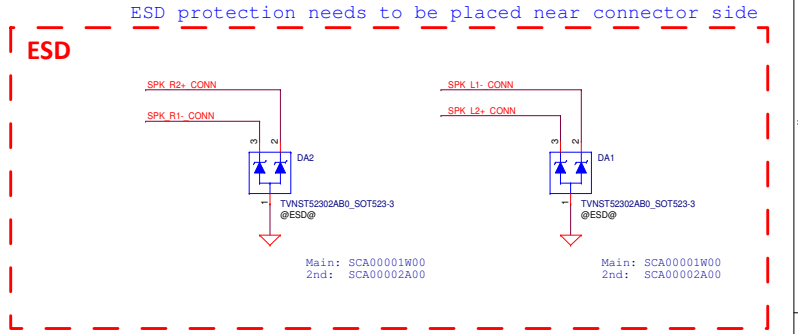
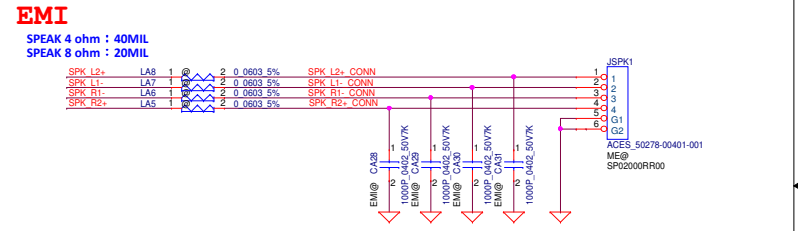
PC Beep



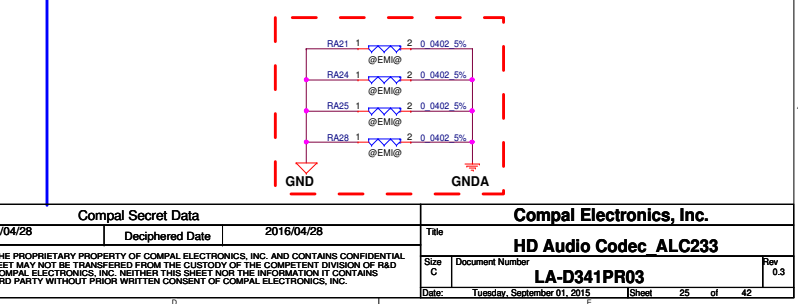
Input



Output

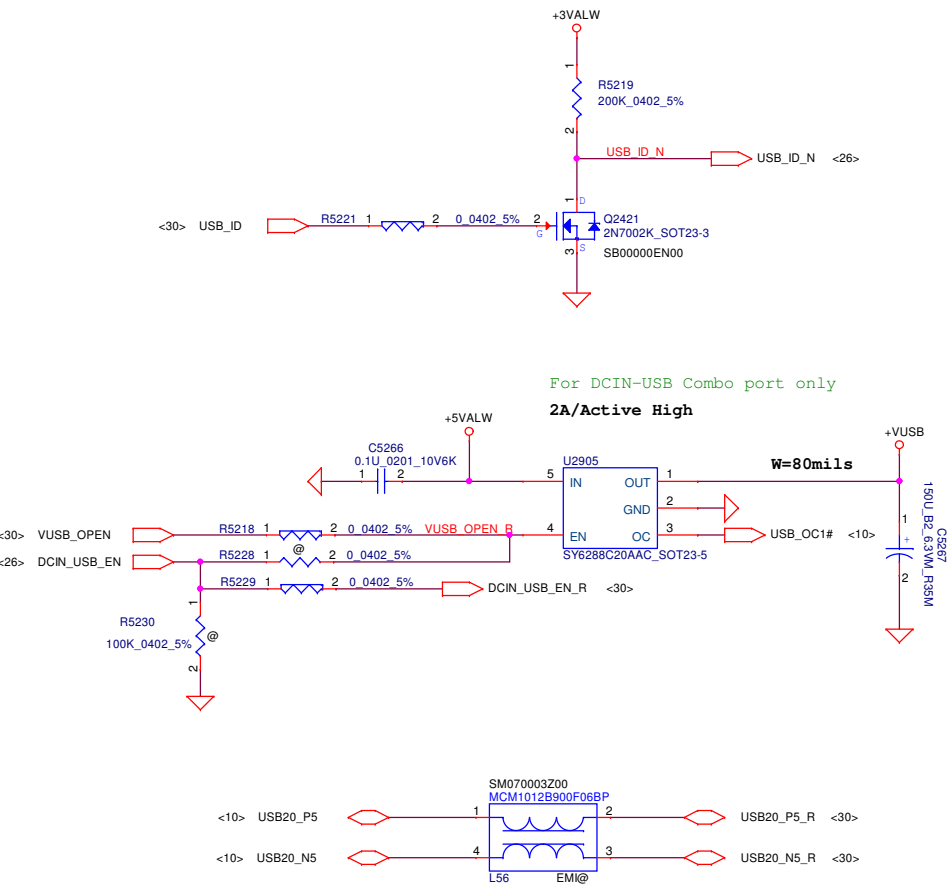


EMI



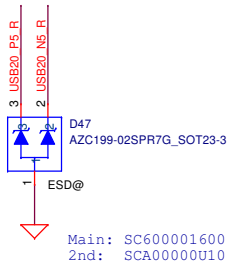
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DCIN-USB PWR SW



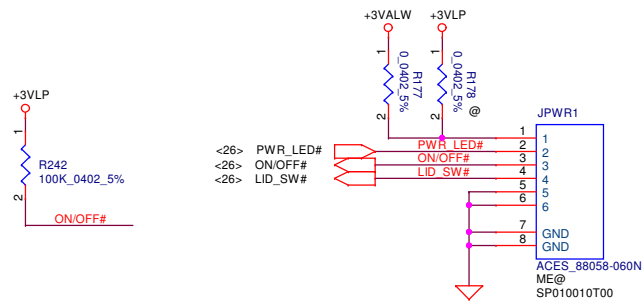
	AC S0	AC S3	AC S5
USB_ID_N	L	L	L
DCIN_USB_EN	L	L	L
VUSB_OPEN	L	L	L
	DC S0	DC S3	DC S5
USB_ID_N	H	H	L
DCIN_USB_EN	H	L	L
VUSB_OPEN	H	H	L
	DC to AC S0	DC to AC S3	DC to AC S5
USB_ID_N	H-->L	H-->L	L-->L
DCIN_USB_EN	H-->L	L-->L	L-->L
VUSB_OPEN	H-->L	H-->L	L-->L
	AC to DC S0	AC to DC S3	AC to DC S5
USB_ID_N	L-->H	L-->H	L-->L
DCIN_USB_EN	L-->H	L-->L	L-->L
VUSB_OPEN	L-->H	L-->H	L-->L

AC to DC S0
When EC get USB_ID_N L--> H, then
DCIN_USB_EN need delay 2's then L-->H

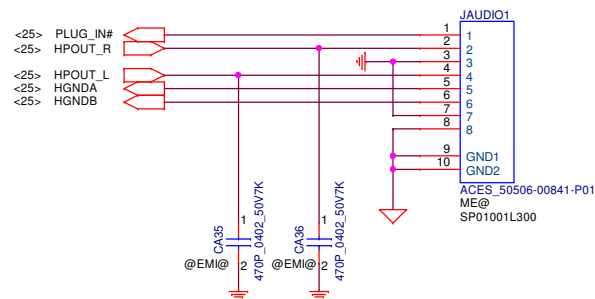


Main: SC600001600
2nd: SCA00000U10

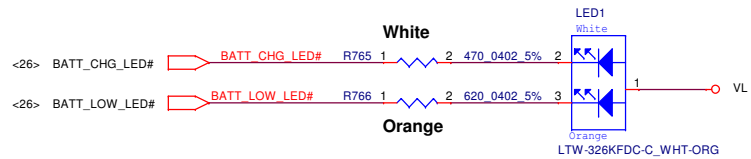
PWR Board



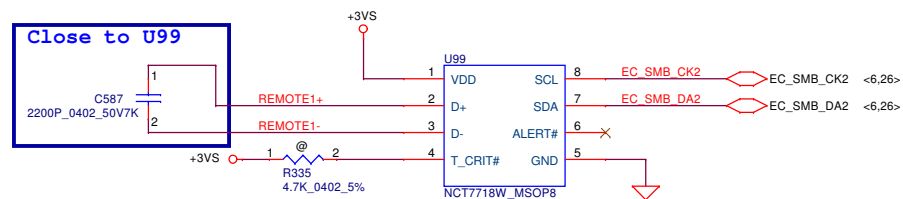
I/O Board



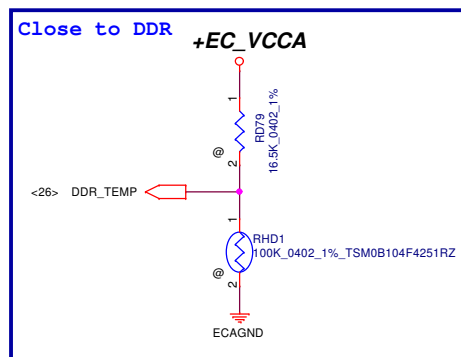
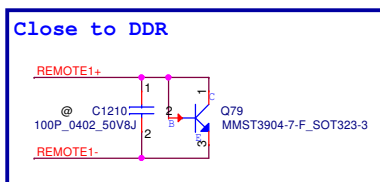
LED



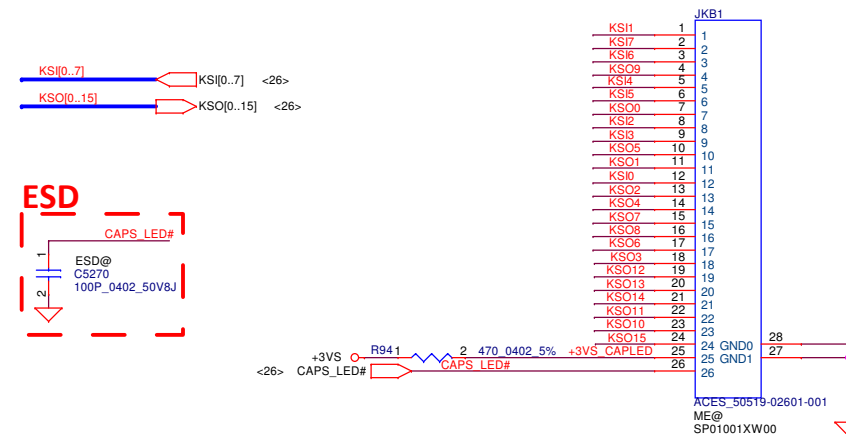
Thermal Sensor



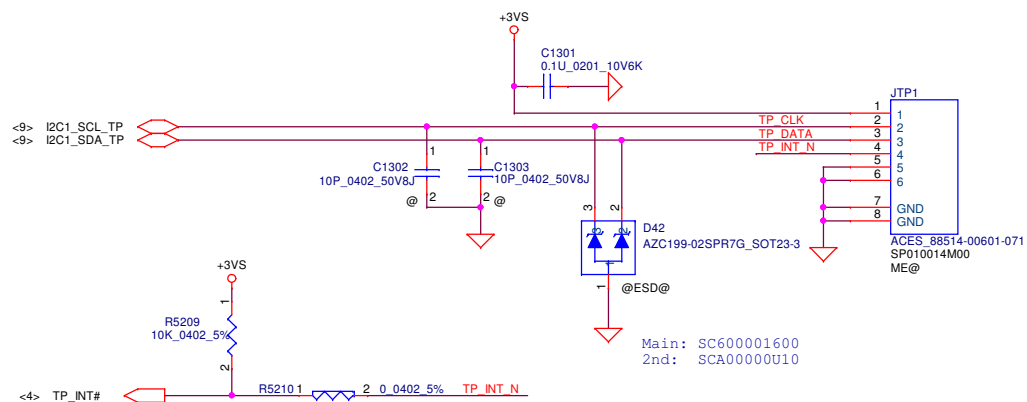
```
REMOTE1+/-:
Trace width/space:10/10 mil
Trace length:<8"
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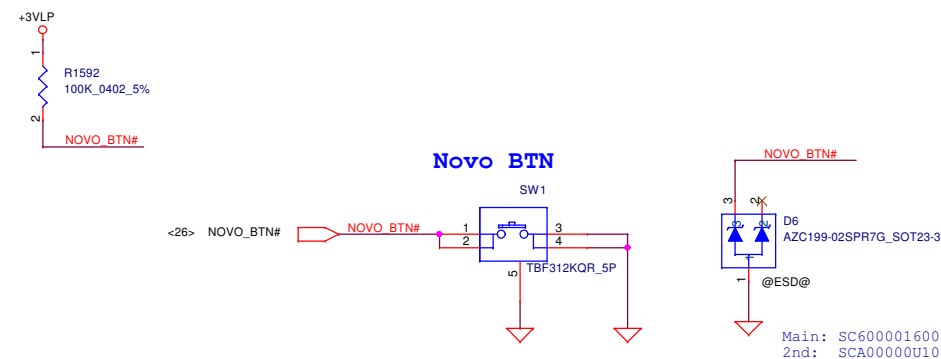
Keyboard



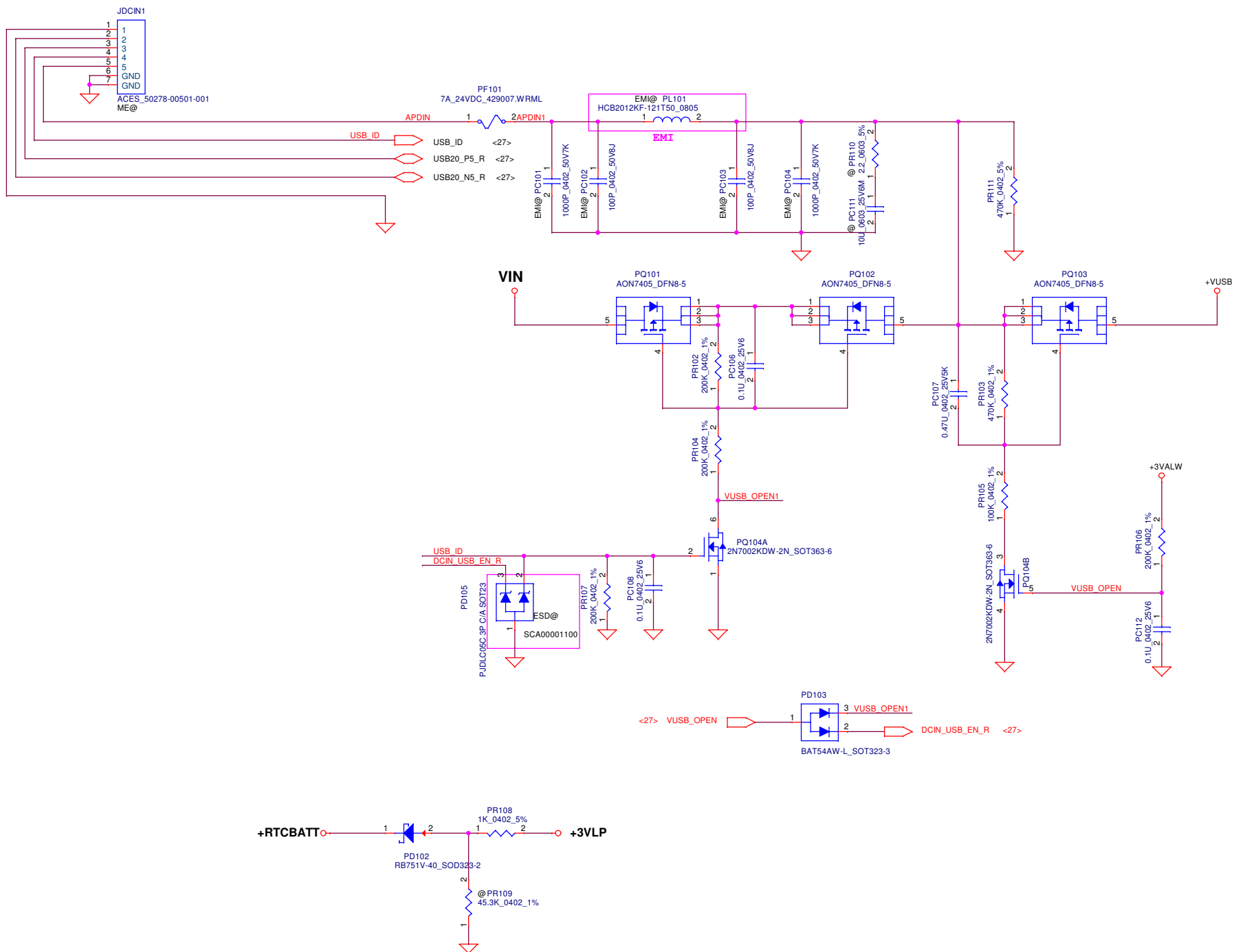
Click Pad



BUTTON



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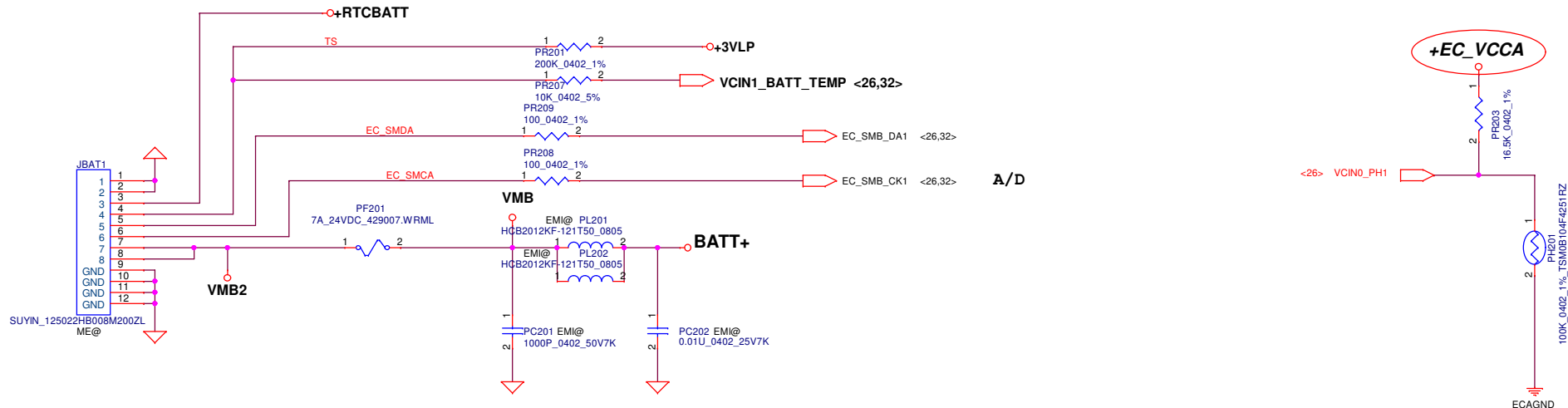


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PH201 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

65W(UMA): 85W active W recovery

20120314
Change to +EC_VCCA from +3VLP



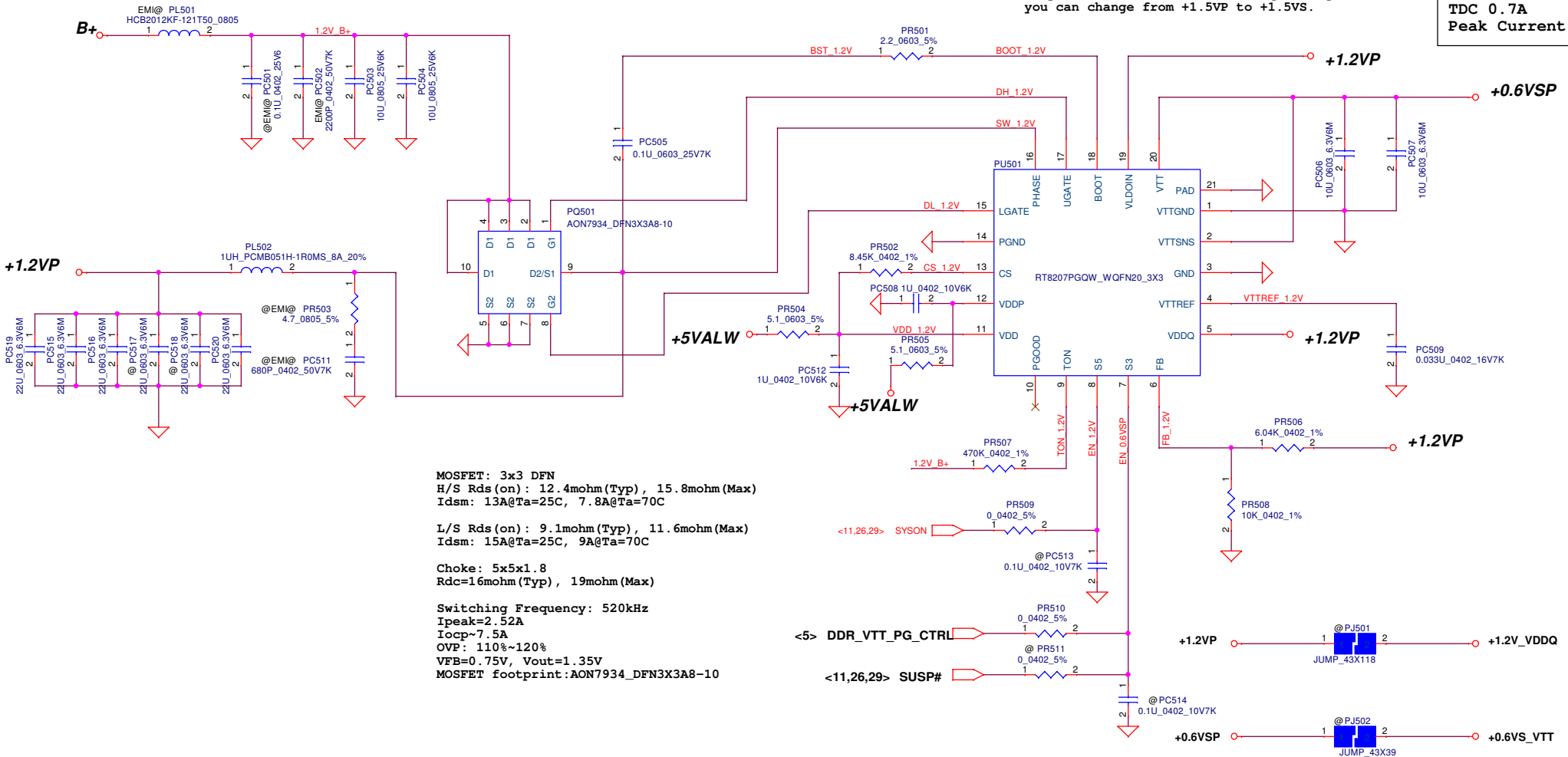
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Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

Pin19 need pull separate from +1.5VP.
If you have +1.5V and +0.75V sequence question,
you can change from +1.5VP to +1.5VS.

0.75Volt +/- 5%
TDC 0.7A
Peak Current 1A

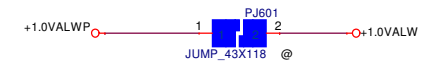
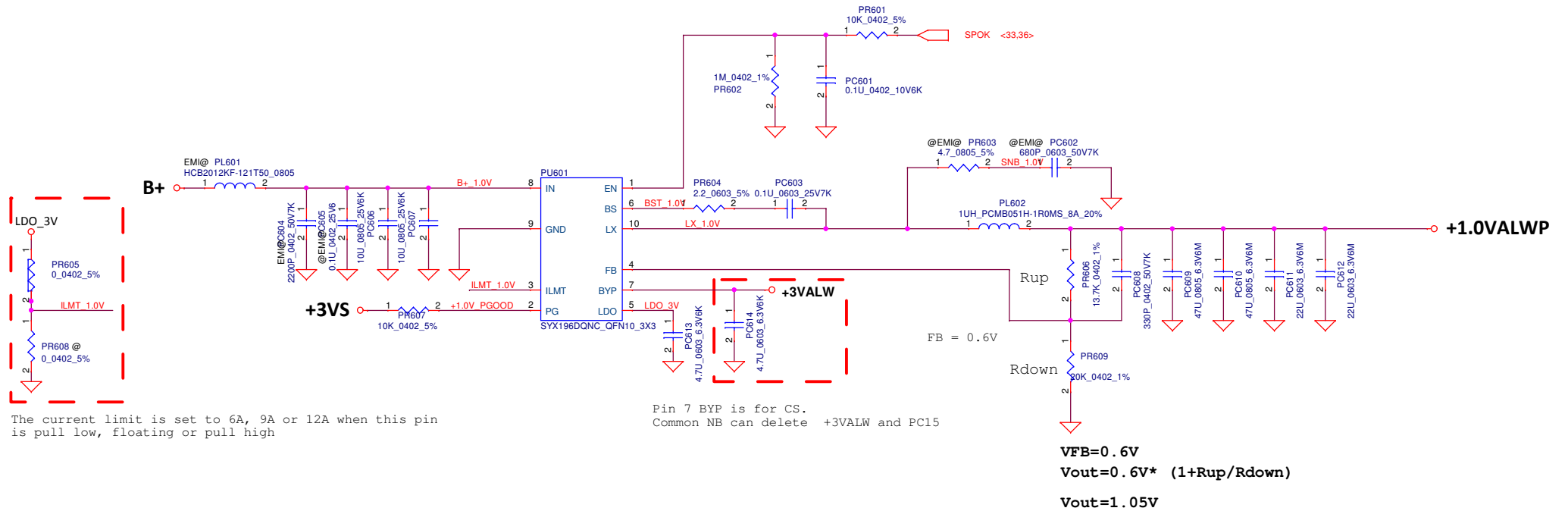


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												3		1		2			

Module model information

SYX196D_V3.mdd

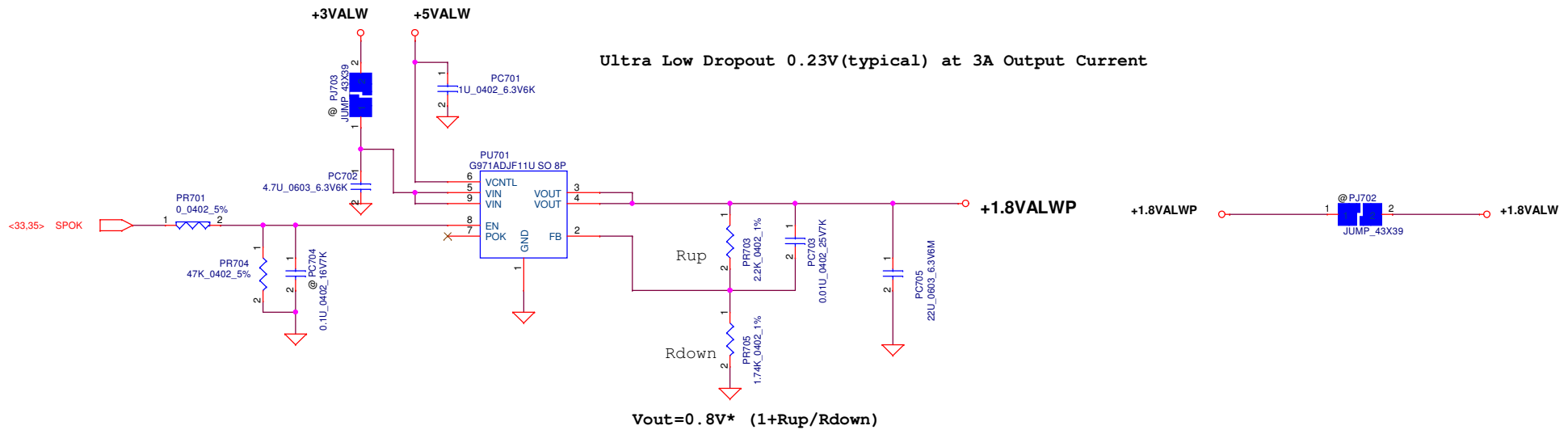
EN pin don't floating
If have pull down resistor at HW side, pls delete PR2



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		Size	Document Number				Rev			
		Custom					0.3			
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Module model information

APL5930_V2.mdd



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IccMAX@SA= 5A
RiccMAX@SA= 15.8K ---->PRI65

RiccMAX@SA= IccMAX*2V/10uA/64A

IOUTSP@SA= 5A
RIOUTSP@SA=31.6K ---->PRI14

RIOUTSP= 2V/(gm*(Rth+RCSSP))*IccMAX*DCR
/(RPHSP+Rth+RCSSP)

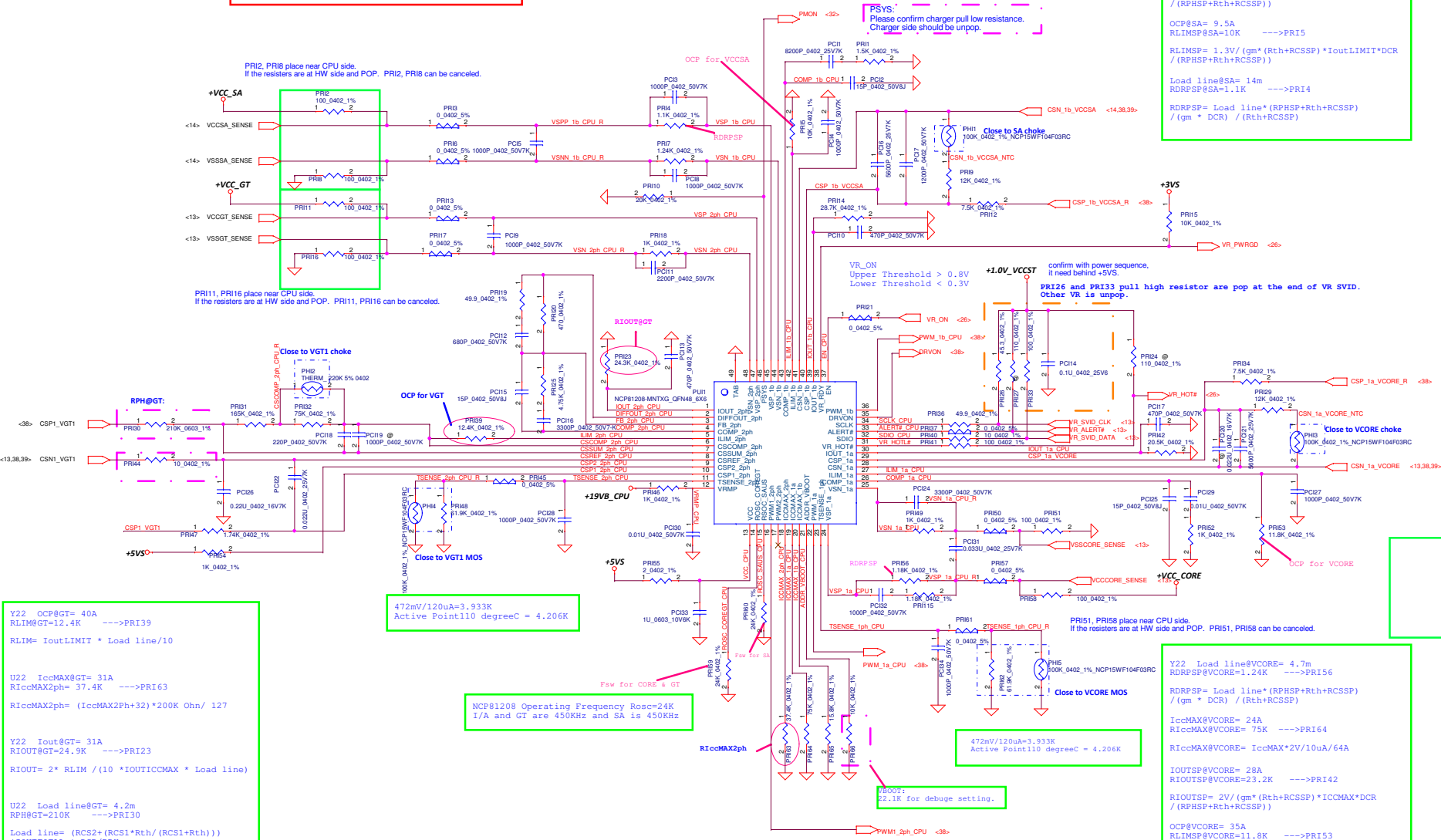
OCP@SA= 9.5A
RLIMSP@SA=10K ---->PRI5

RLIMSP= 1.3V/(gm*(Rth+RCSSP))*IoutLIMIT
/(RPHSP+Rth+RCSSP)

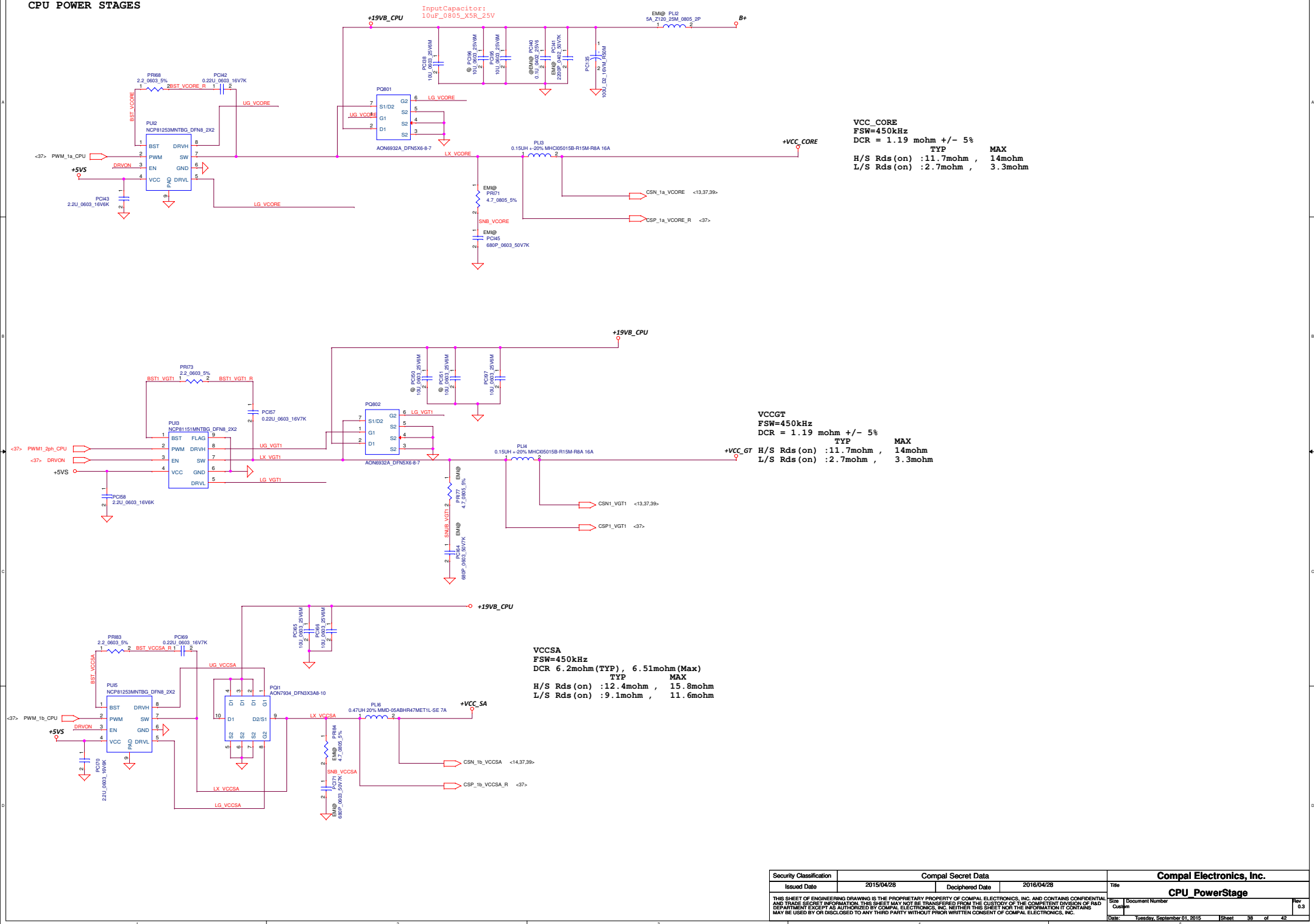
Load line@SA= 14m
RDRSP@SA=1.1K ---->PRI4

RDRSP= Load line/(RPHSP+Rth+RCSSP)
/(gm * DCR) /(Rth+RCSSP)

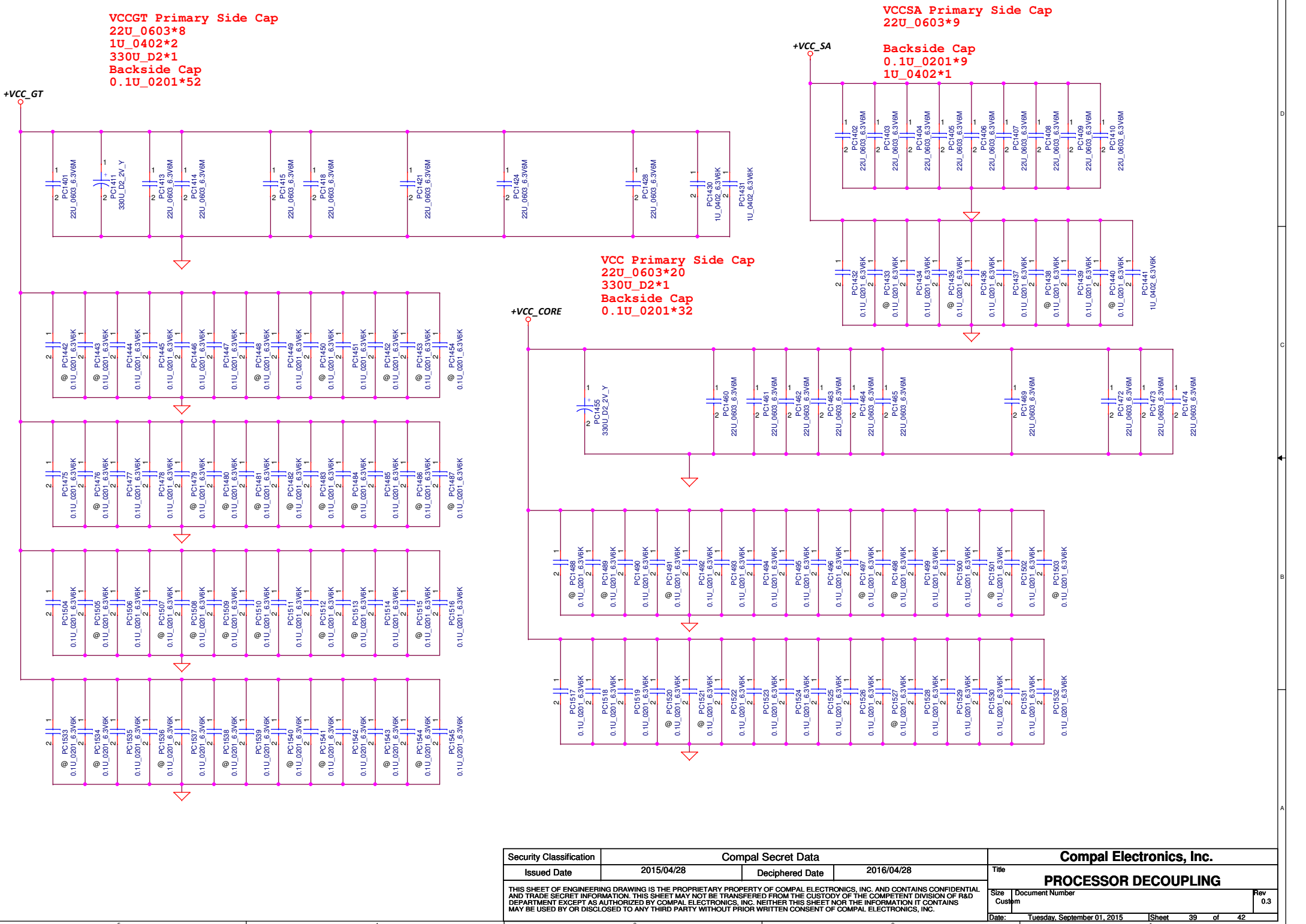
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CPU POWER STAGES



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Version change list (P.I.R. List)

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for PWR

Item	Reason for change	PAGE	Modify List	Date	Phase
2015.05.12	P37-PWR-CPU_CORE change PCI11 from 1000p to 2200p for FAE's request.				
2015.05.12	P37-PWR-CPU_CORE change PCI26 from 0.1U to 0.22U for FAE's request.				
2015.05.12	P37-PWR-CPU_CORE change PRI14 from 31.6k to 30.1k for FAE's request.				
2015.05.12	P37-PWR-CPU_CORE change PRI20 from 1k to 470 for FAE's request.				
2015.05.18	P30-PWR-DCIN / Vin Detector add PR108 and PR109.				
2015.06.03	P32-PWR_Charger PR318				
2015.06.03	P30-PWR-DCIN / Vin Detector SB00000EO10(X1) change to SB00000EO00				
2015.06.03	P33-PWR-3VALW/5VALW SH000013500(X1) change to SH000015A00				
2015.06.03	P34-PWR-1.2VP/0.6VS & P35-PWR-1.0VALW SH00000X400(X1) change to SH000014Y00				
2015.06.05	P39-PWR-PROCESSOR DECOUPLING Capacitor 32+4+10 follow Paganini				
2015.06.08	P36-PWR-1.8VALW change PR701 from 100k to 0				
2015.06.11	P32-PWR_Charger change PU301 from BQ24777(SA000078H00) to BQ24770(SA00007XL00)				
2015.06.25	P37-PWR-CPU_CORE change PRI12&PRI34 from 0603 to 0402				
2015.06.25	P38-PWR_CPU_PowerStage add @PCI96,@PCI51				
2015.06.25	P32-PWR_Charger @PC318,@PC319,@PC324				
2015.07.06	P32-PWR_Charger PC318,PC319,PC320 & ADD PC331				
2015.07.06	P39-PWR-PROCESSOR DECOUPLING Remover PC1412,1416,1417,1419,1420,1422,1423,1425,1426,1427,1429 & change PC1411 from 22U to 330U				
2015.07.06	P39-PWR-PROCESSOR DECOUPLING Remover PC1456,1457,1458,1459,1466,1467,1468,1470,1471 & change PC1455 from 22U to 330U				
2015.07.07	P37-PWR-CPU_CORE change PRI7 from 1k to 1.24k, PCI8 from 1000P to 3300P, PCI6 from 4700P to 5600P, PRI14 from 30.1k to 28.7k, PRI23 from 24.9k to 24.3k, PCI16 from 2200p to 3300p, PCI21 from 6800p to 5600p, PCI42 from 23.2k to 20.5k, PCI56,PCI115 from 1.24k to 1.18k,				
2015.07.07	P32-PWR_Charger PR321,PR322 change to R-short				
2015.07.07	P35-PWR-1.0VALW PR605 change to R-short				
2015.07.07	P36-PWR-1.8VALW PR701 change to R-short				
2015.07.07	P37-PWR-CPU_CORE PRI3 PRI6 PRI13 PRI17 PRI45 PRI61 change to R-short				
2015.07.09	P35-PWR-1.0VALW change PR601 from 0 to 10k, PC601 from 0.22U to 0.1U				
2015.07.09	P36-PWR-1.8VALW Unmount PC704				
2015.07.15	P32-PWR_Charger PL302 from 2.2U to 3.3UH				
2015.07.21	P37-PWR-CPU_CORE change PCI29 from 1500p to 10n(0.01U) for FAE's request.				
2015.07.21	P37-PWR-CPU_COREchange PRI52 from 2.49k to 1k for FAE's request.				
2015.07.21	P37-PWR-CPU_CORE change PCI31 from 1000p to 33n(0.033U) for FAE's request.				
2015.07.21	P38-PWR-CPU_PowerStage Assemble PRI71,PCI45,PRI77,PCI64,PRI84,PCI71				
2015.08.13	P38-PWR-CPU_PowerStage SH000015G10(X1) change to SH000015G20				
2015.08.17	P33-PWR-3VALW/5VALW PR407 change to R-short				
2015.08.17	P37-PWR-CPU_CORE PRI21 PRI37 PRI50 PRI57 change to R-short				
2015.08.18	P33-PWR-3VALW/5VALW Add @PC430				

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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase	Verify
1	Initial Schematic			2015/05/29	EVT	
2	+RTCBATT voltage	12	Change RC39 form 806 ohm to 0 ohm	2015/06/02	EVT	
3	EC CLEAR CMOS follow normal design	08	ADD RC10 to 0 ohm, DEL QC7/RC8	2015/06/03	EVT	
4	Modify +1.8V_MEM curcuit	29	Change U8 to SOT23-3 , Add R93/C93	2015/06/23	EVT	
5	SW1	28	Change SW1 footprint to SN100008A00	2015/06/24	EVT	
6	UD1/UD2/UD3/UD4	18	Change footprint to H9CCNNN8JTMLAR-NTM_FBGA_178P-S	2015/06/26	EVT	
7	Add for ESD common design	27	ADD D47 to DC-IN USB	2015/06/26	EVT	
8	Del SOC XDP test point	04	Del TC51/TC52/TC53/TC54/TC55	2015/06/29	EVT	
9	Change RA30/RA31 for EMI request	25	Change RA30/RA31 form R-short ohm to 0 ohm	2015/06/26	EVT	
10	Change for ESD common design	24	Change D44/D45 to ESD@	2015/07/02	EVT	
11	DMIC_CLK Change to bead	25	Rmove RA31 , ADD LA31	2015/07/06	EVT	
12	Reserve 0603 R-short for RF	12	ADD RC156/RC166 to R-short	2015/07/06	EVT	
13	EC CLEAR CMOS follow normal design	08	ADD QC7/RC8 , DEL RC10	2015/07/09	EVT	
14	Disable PLTRST Buffer	08	ADD RC90 , DEL UC3/CC10/RC16	2015/07/15	EVT	
15	+1.8V_MEM Sequence	29	ADD R93 to 10K ohm , C93 to 0.1uF	2015/07/15	EVT	
16	+1.8VS Sequence	11	ADD RC223 to 100K ohm , CC29 to 0.1uF	2015/07/15	EVT	
17	24M Crystal tunning	08	Change CC8/CC9 from 18pF to 15pF	2015/07/15	EVT	
18	32.768K Crystal tunning	08	Change CC11/CC12 from 18pF to 8.2pF	2015/07/15	EVT	
19	JHDMI1	22	Change JHDMI1 footprint	2015/08/14	DVT	
20	RF 5GHz noise	12	Change RC156 to LC156	2015/08/19	DVT	
21	RF 5GHz noise	12	Change RC156 to LC156	2015/08/19	DVT	
22	POWER LED strip 3VALW/3VLP	27	Add R177 & R178 to 0 ohm	2015/08/20	DVT	
23	RF 5GHz noise	12	Reserve RC152/RC159 to 0 ohm for RF	2015/08/24	DVT	

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[Power ON Sequence] (TBC)

